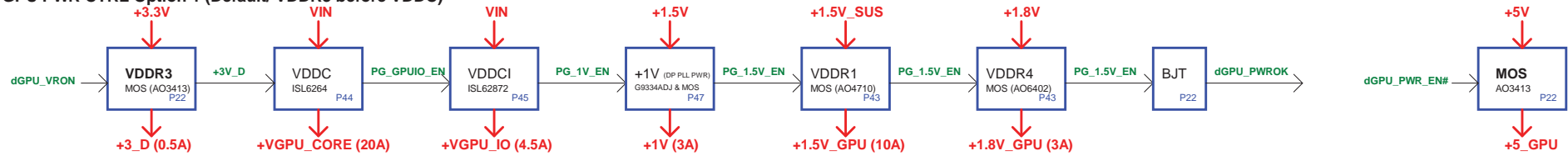
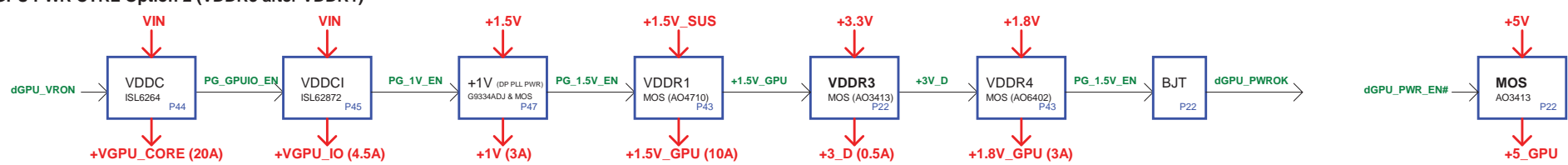


GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



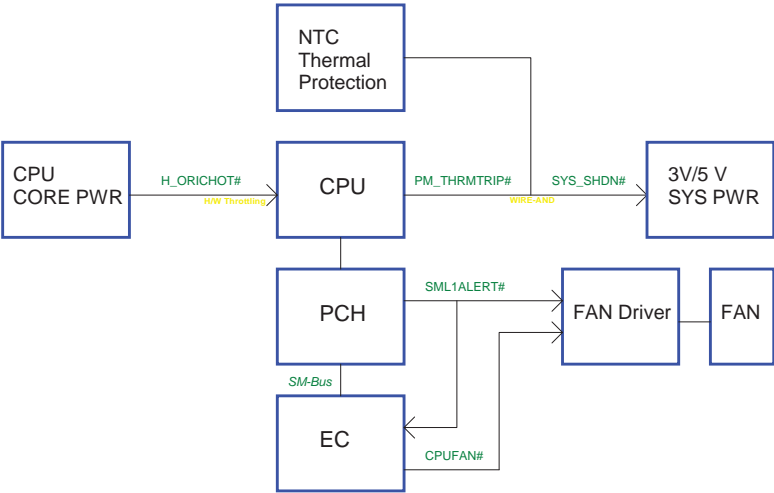
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)

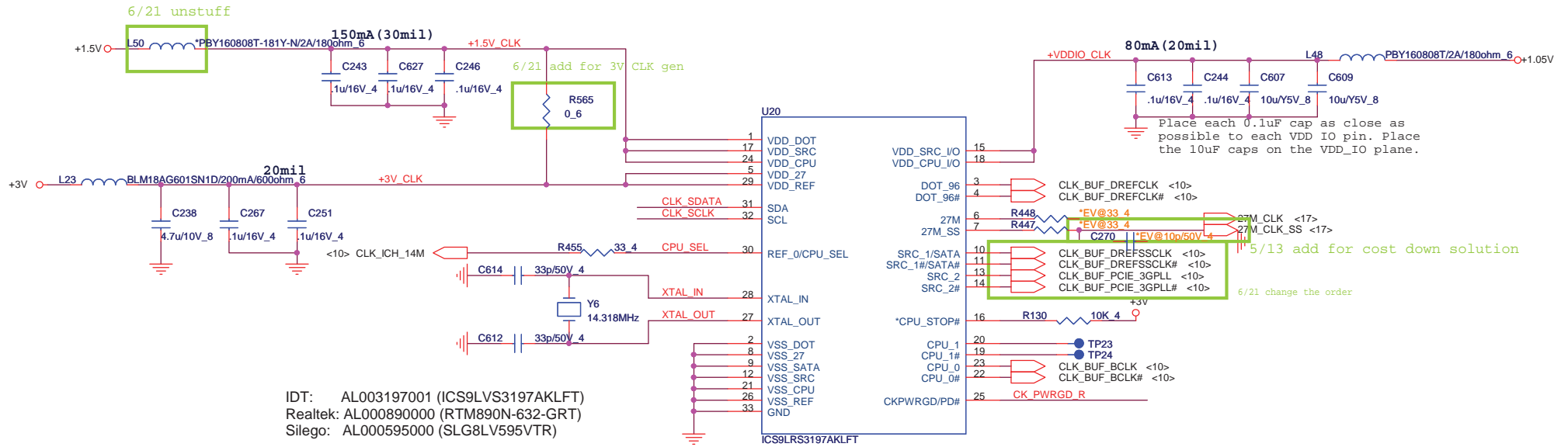


Power States

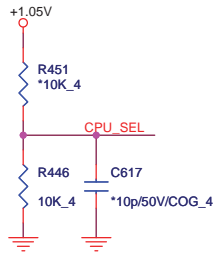
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



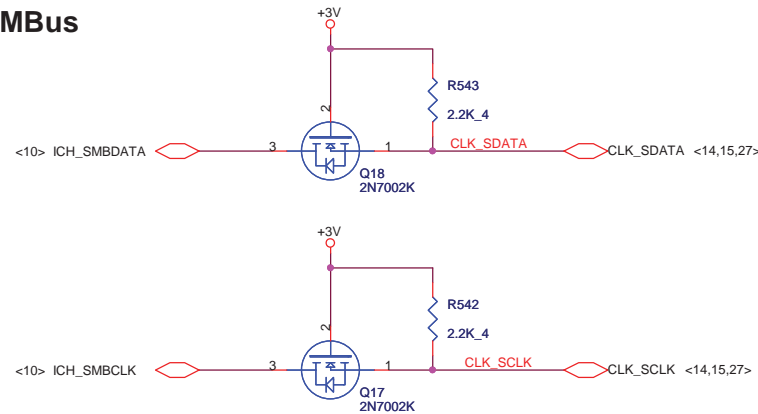


CPU_CLK select

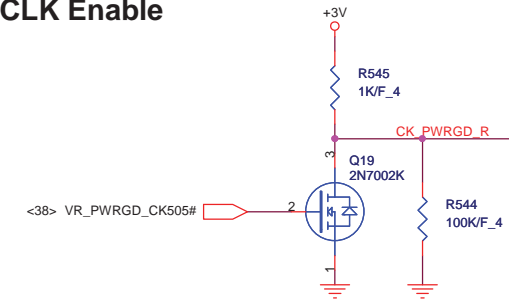


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



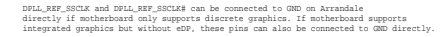
CLK Enable



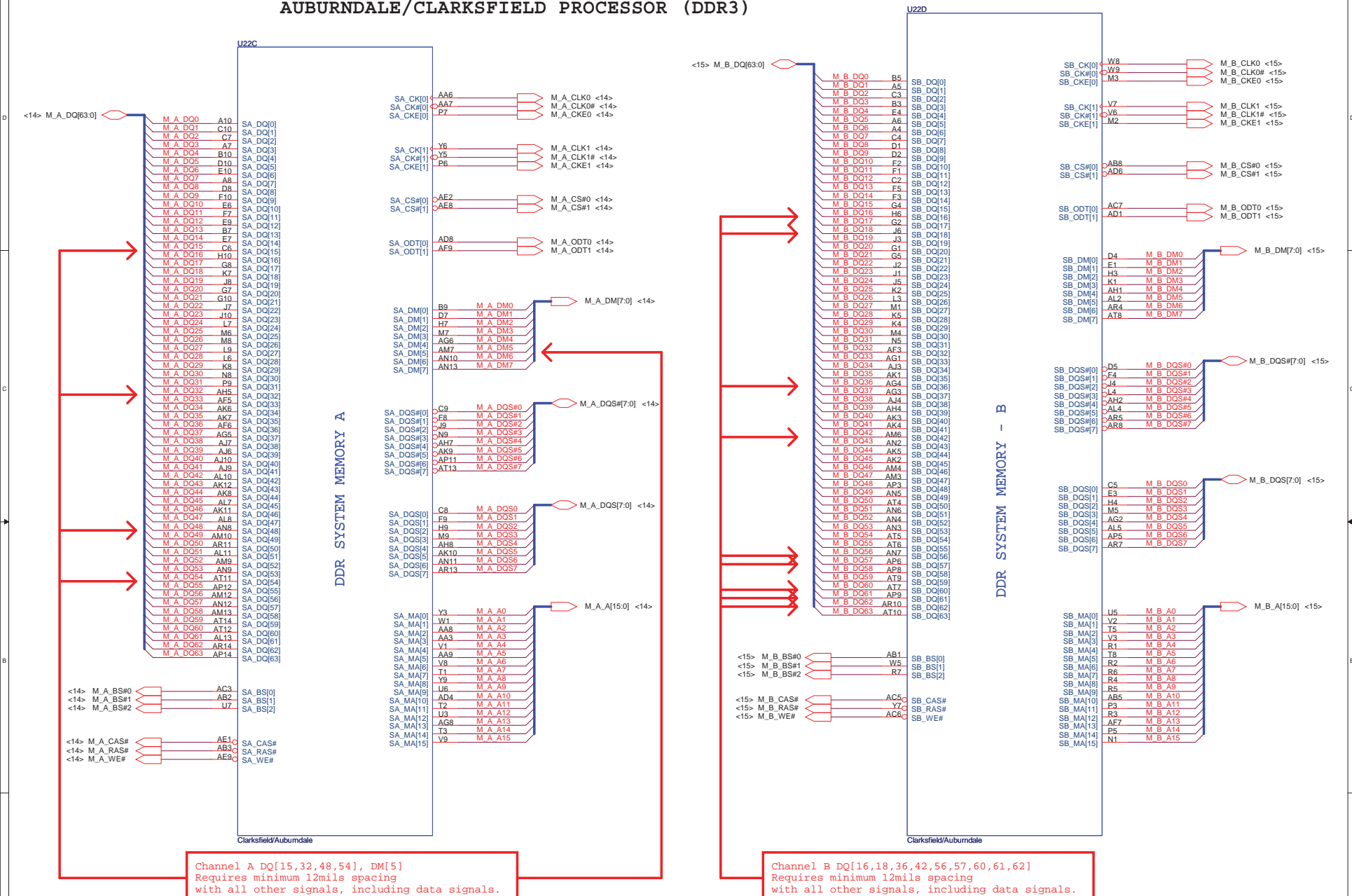
Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	Clock Generator	1A
Date:	Tuesday, June 22, 2010	Sheet 3 of 45

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

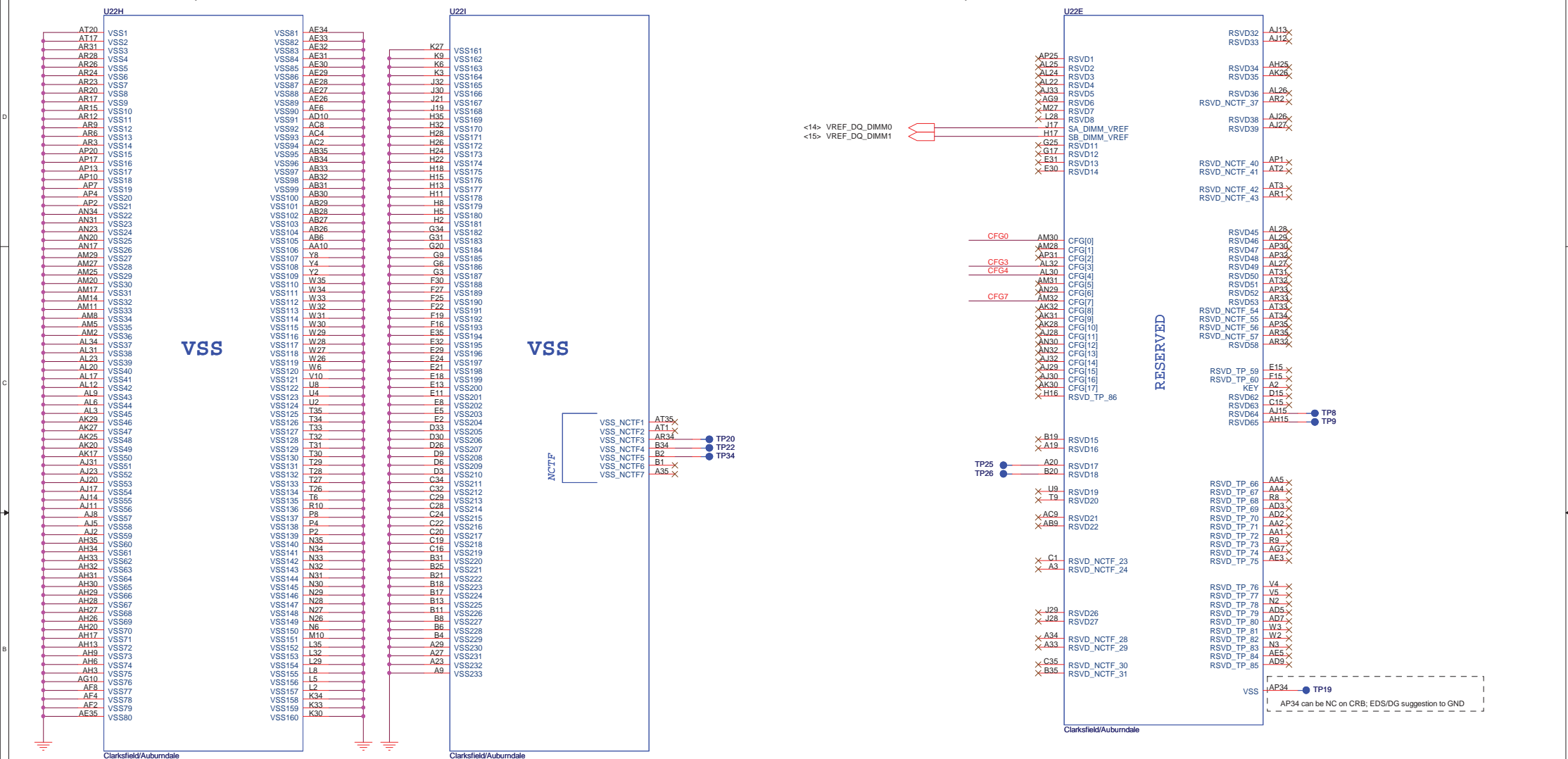
[illegible]

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)

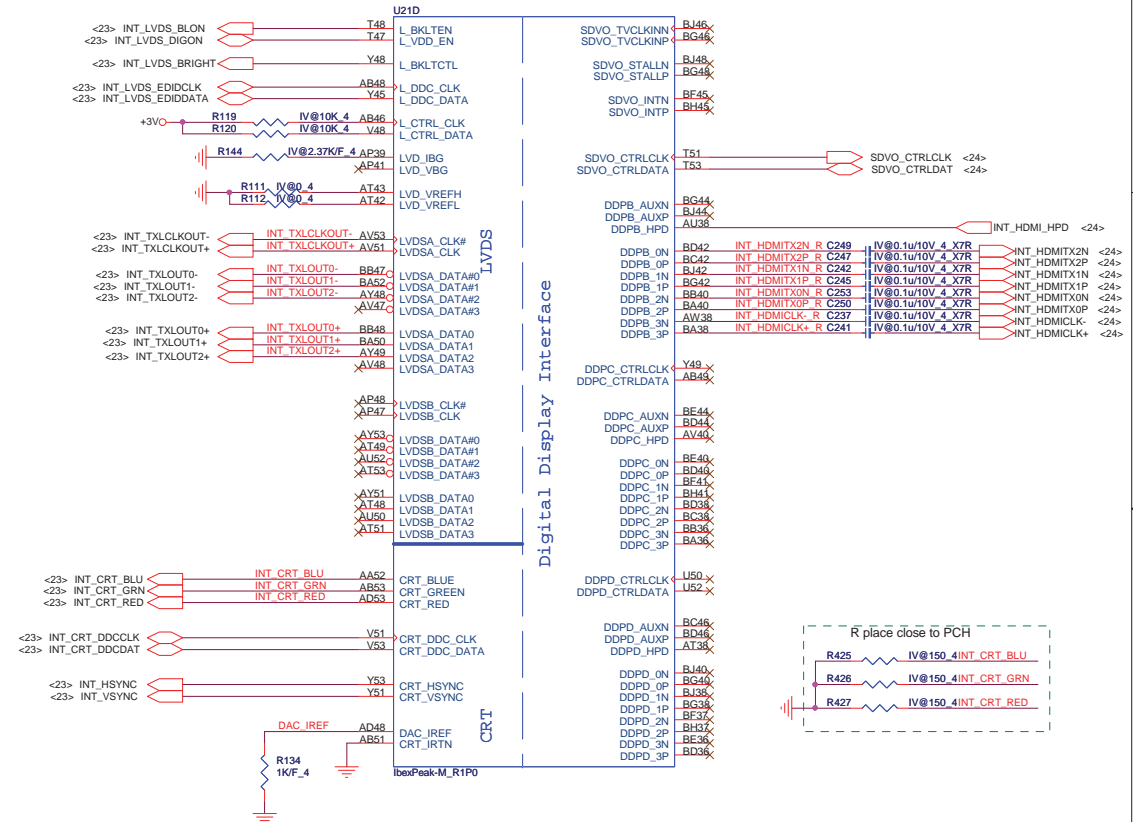


Processor Strapping

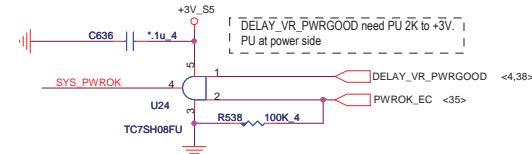
	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R128 ~3.01K NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R125 ~3.01K/F 4
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R127 ~3.01K
T h b e t p B A				CFG7 R126 ~3.01K/F 4


AC-coupling CAP place close to PCH

IBEX PEAK-M (LVDS, DDI)

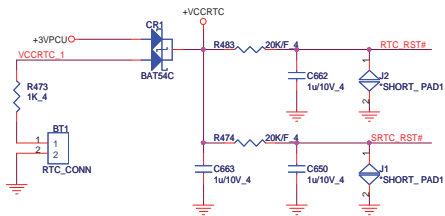


System PWR_OK



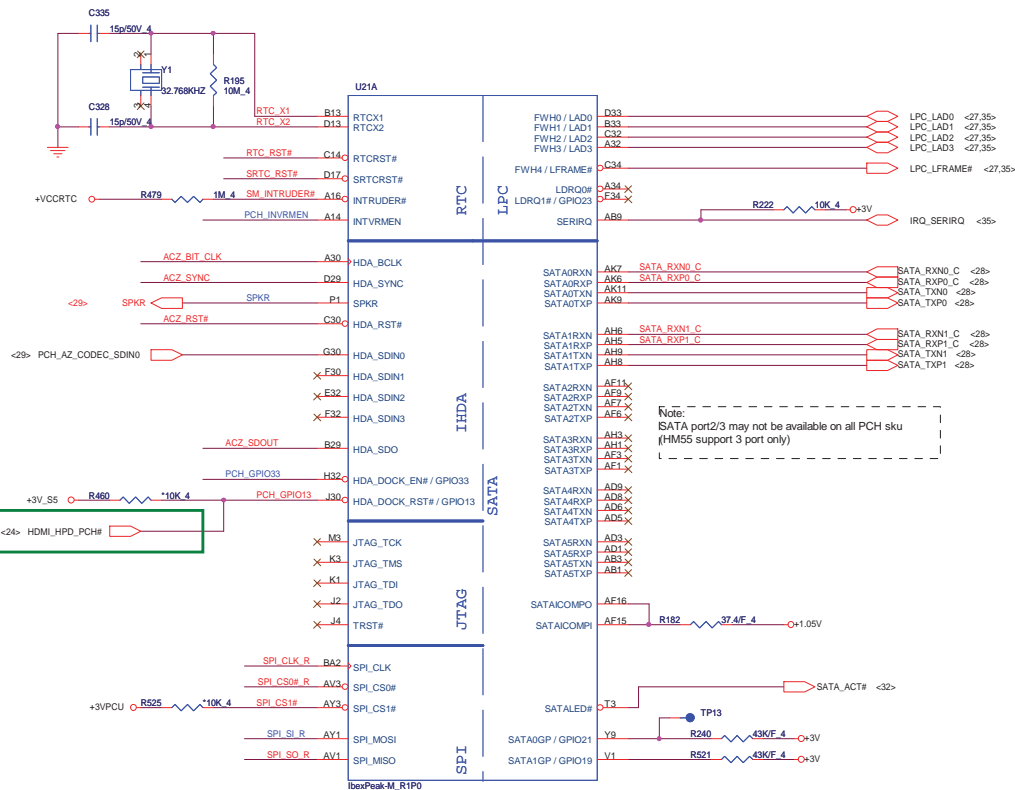
 Quanta Computer Inc. PROJECT : ZQ9		
Size	Document Number IBEX PEAK-M 1/6	Rev 1A
Date:	Tuesday, June 22, 2010	Sheet 8 of 45

RTC Circuitry



HDA_SYNC (PCH strap pin)

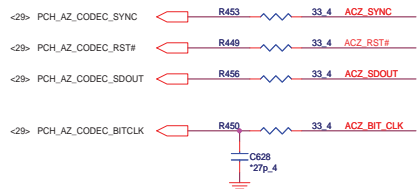
Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V



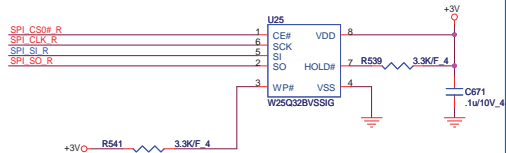
PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R489 330K 6 PCH INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R540 1K 4 SPI SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R532 1K 4 SPKR
HDA_DOCK#EN /GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R184 1K 4 R146 10K 4
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	R129 1K 4 R122 1K 4 R131 1K 4
GNT2# /GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	<10> PWM_SELECT# R158 1K 4
GNT3# /GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	<10> PCI_GNT3# R421 10K 4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	<10> NV_ALE R202 1K 4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	<10> NV_CLE R206 1K 4 +1.8V
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	SV_GPIO8 R204 10K 4 +3V_S5 R203 1K 4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	CR_WAKE# R244 1K 4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	<11> PCH_GPIO27 R221 10K 4

HDA Bus



PCH SPI



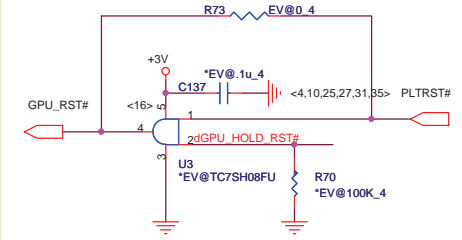


IBEX PEAK-M (GPIO, VSS_NCTF, RSVD)

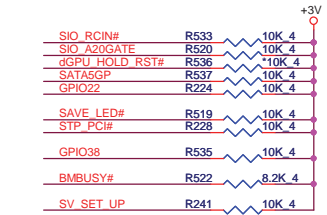
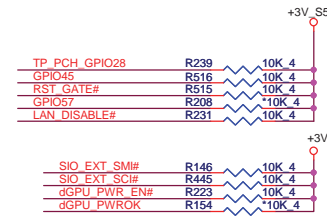


GPU_RST#

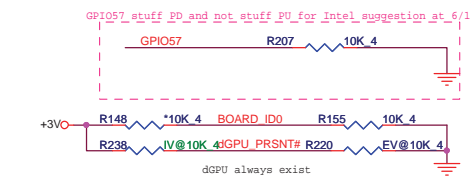
5/18 change for discrete only



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------



dGPU always exist

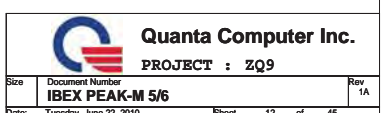
5/18 separate for 14" & 15"

BOARD_ID0	High = 15"
	Low = 14"
RSV_GPIO8	High = Disable
	Low = Enable

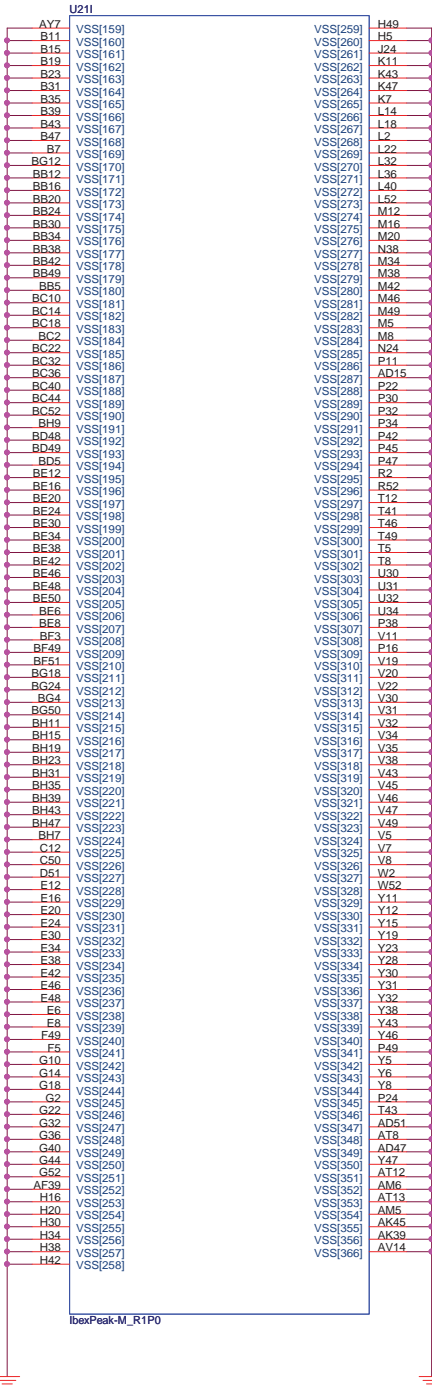
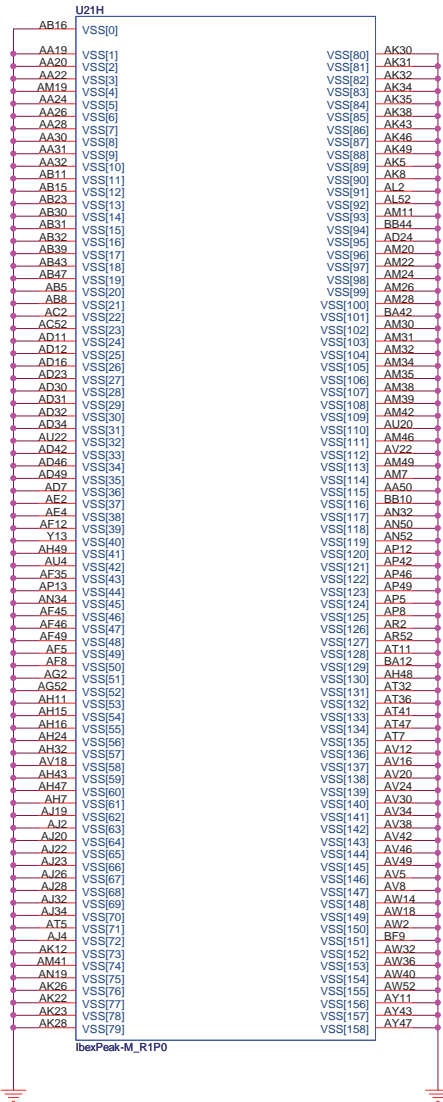


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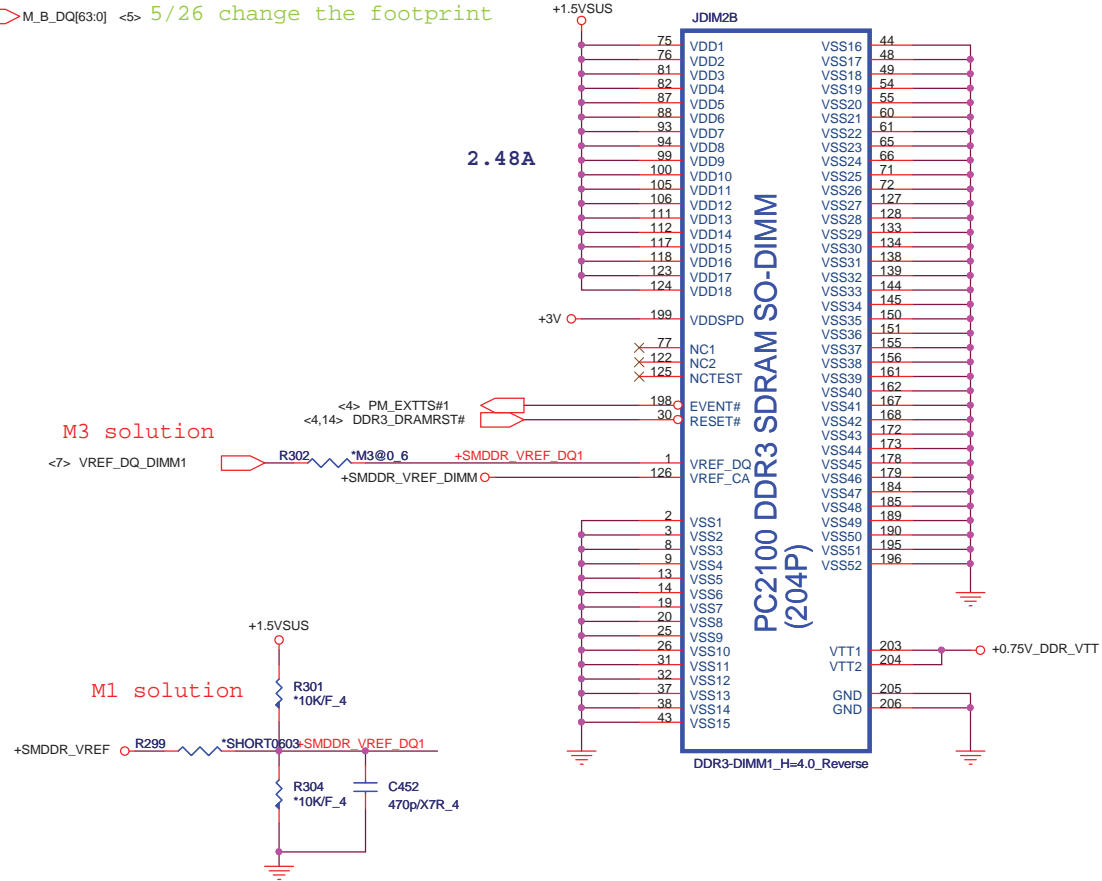
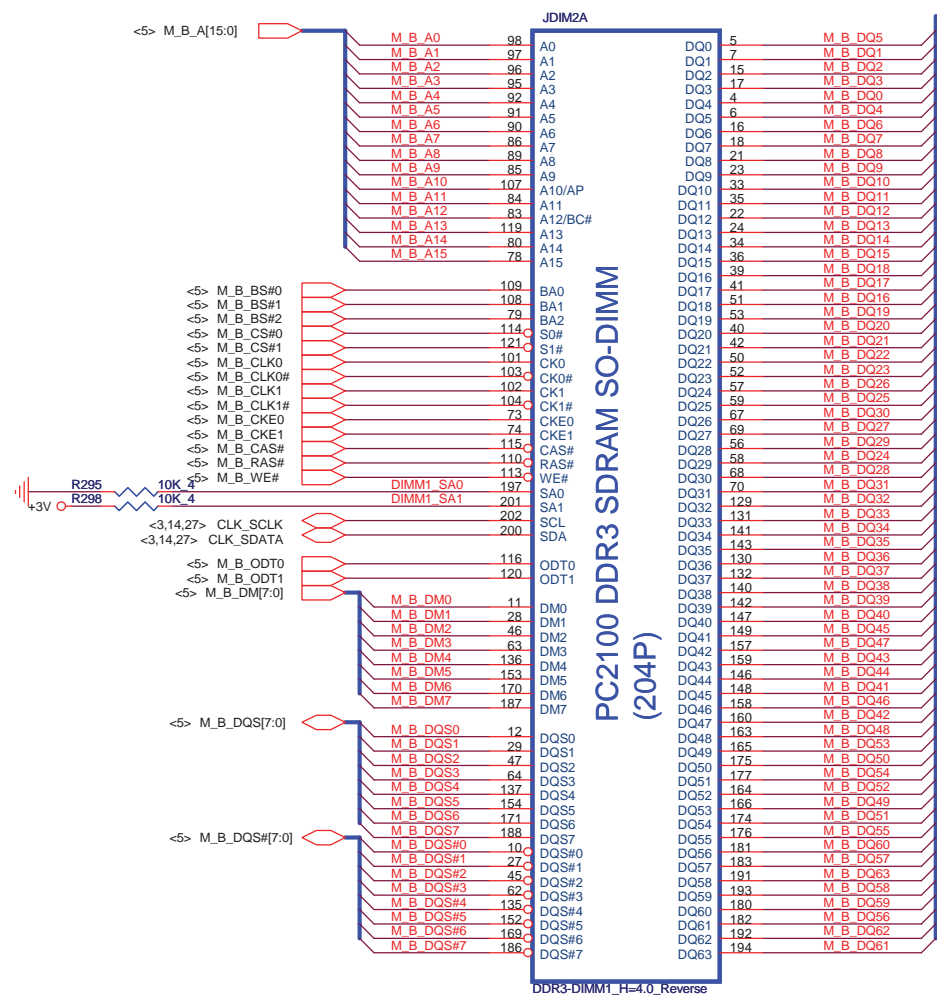
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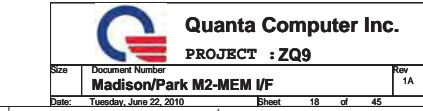


IBEX PEAK-M (GND)

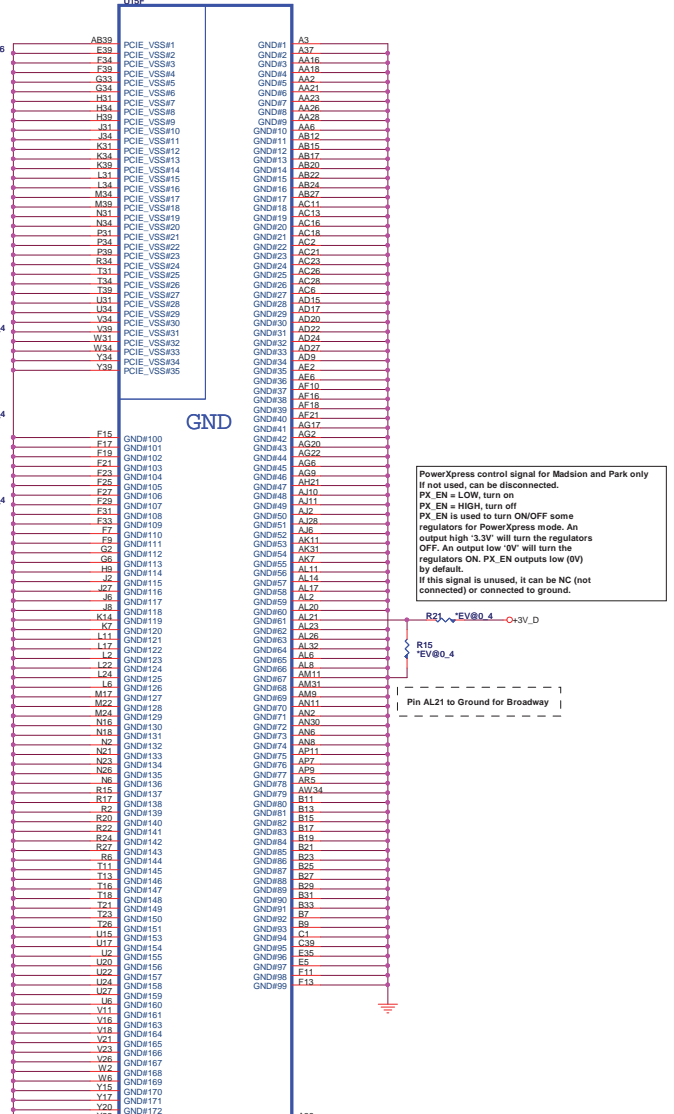
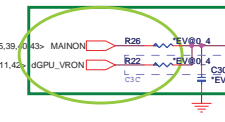
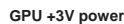
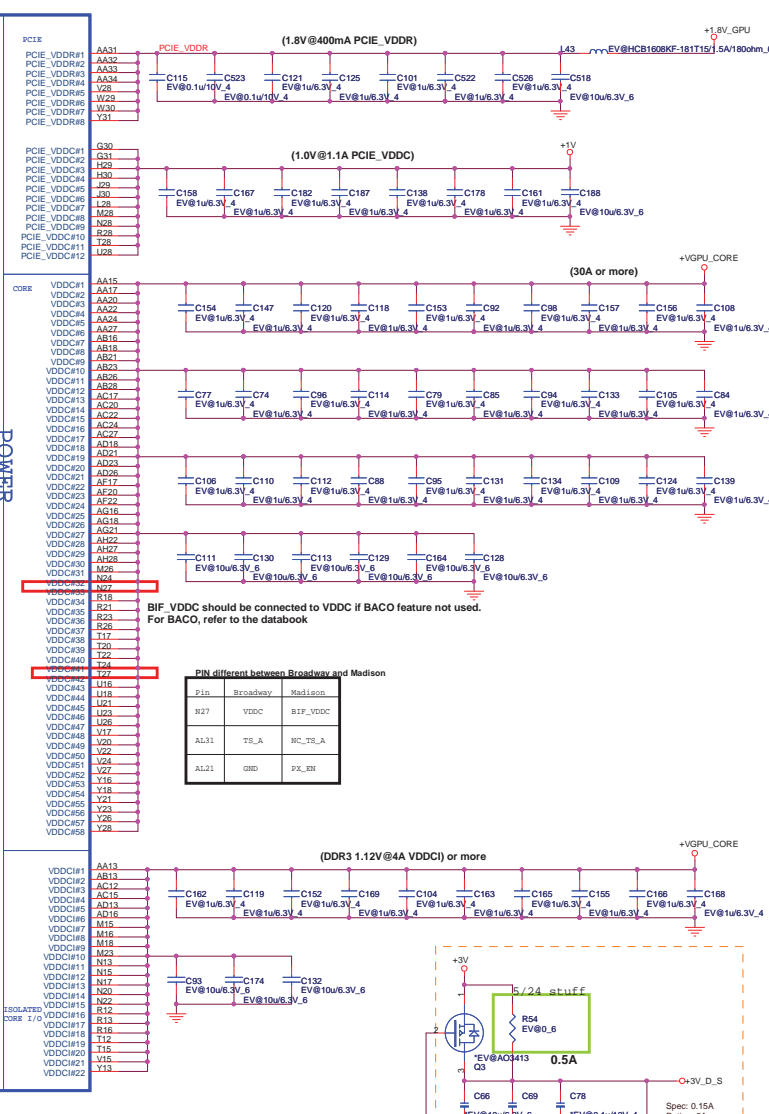
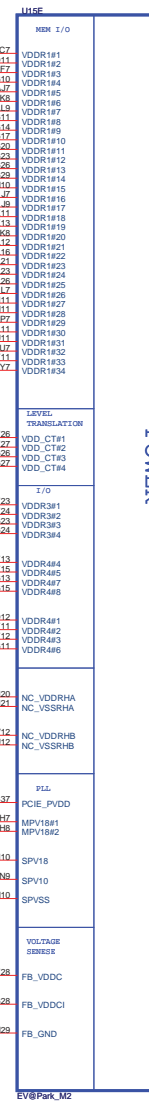
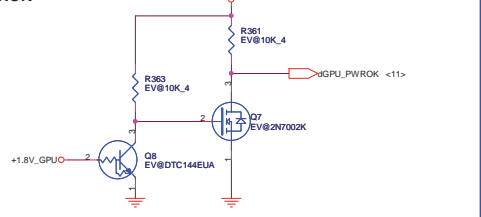
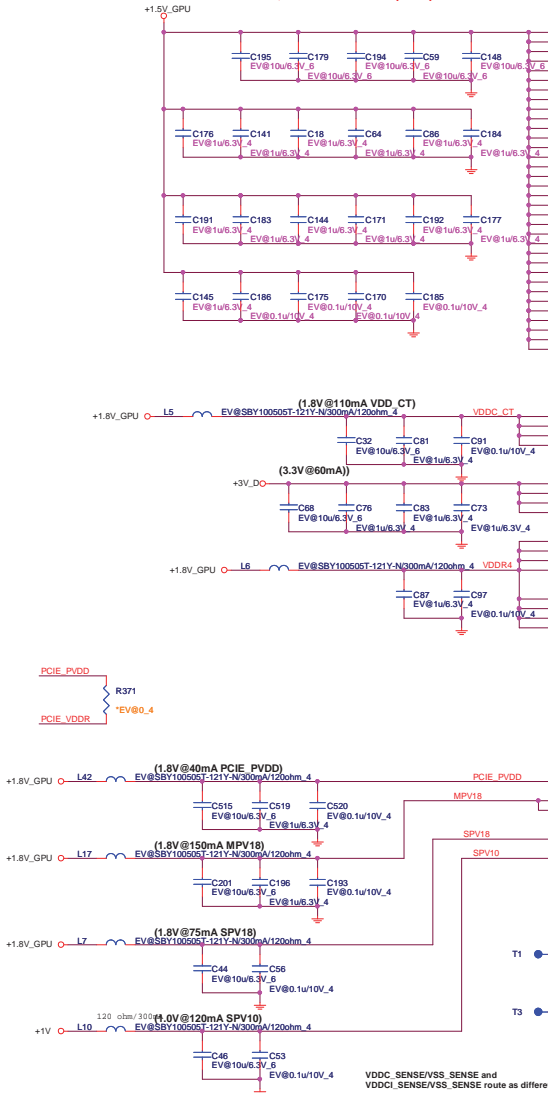


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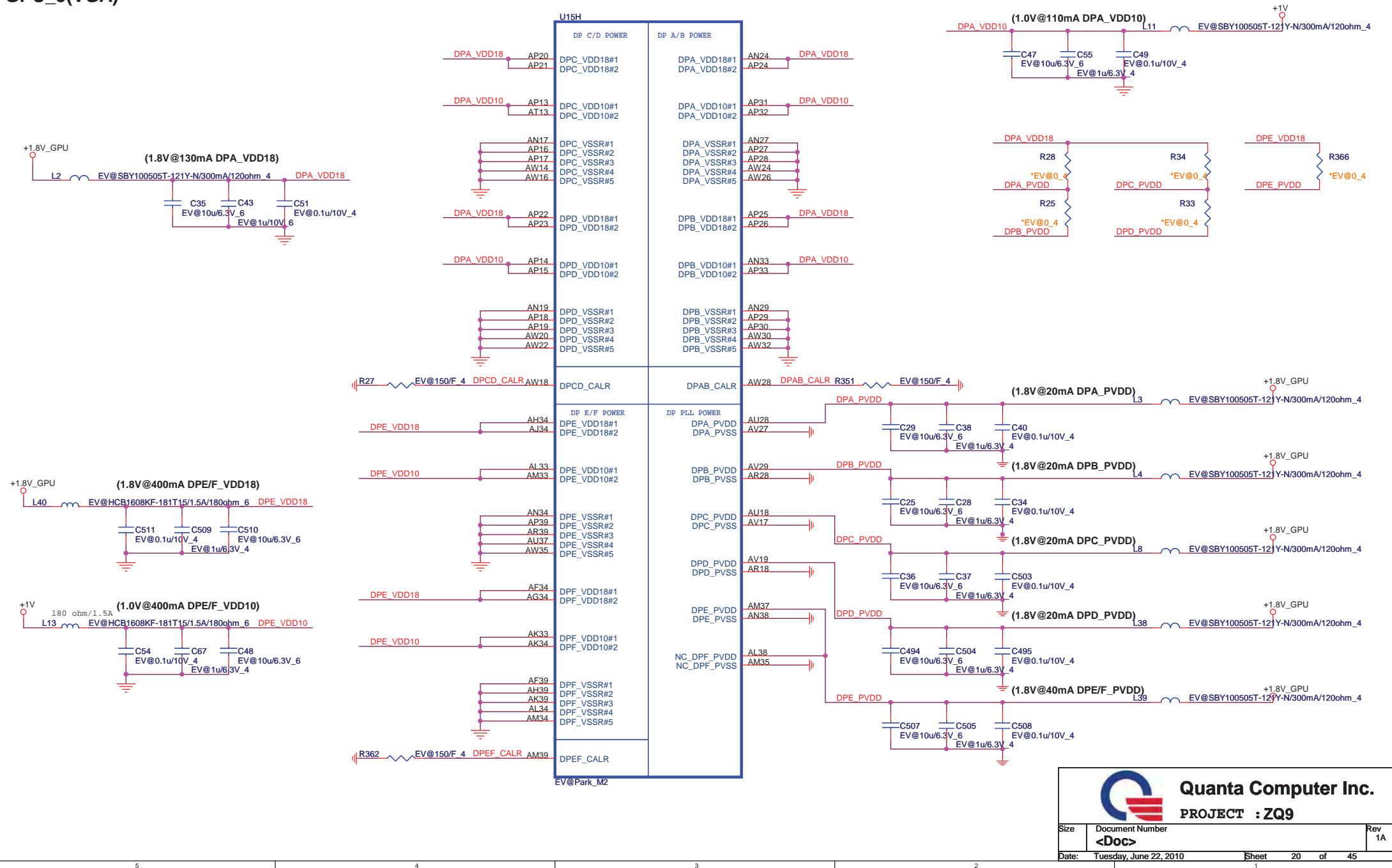
GPU_4(VGA)



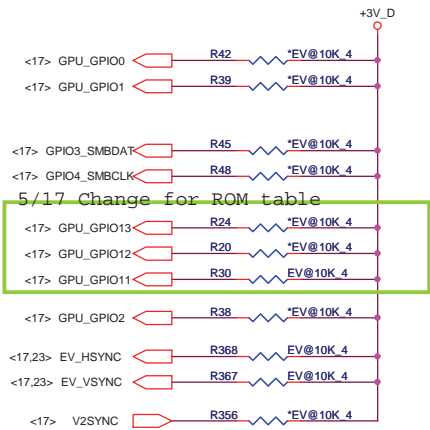
PowerXpress control signal for Madsion and Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some
regulators for PowerXpress mode. An
output high '3.3V' will turn the regulators
OFF. An output low '0V' will turn the
regulators ON. PX_EN outputs low (0V)
by default.
If this signal is unused, it can be NC (not
connected) or connected to ground.

Pin AL21 to Ground for Broadway

GPU_5(VGA)



PIN STRAPS(VGA)



Size of the primary memory apertures	GPIO[13:11]
128 MB	000
256MB	001
64 MB	010
32 MB	011
More than 512 MB	Not Supported

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0	
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIe DEVICE AS 2.5GT/S CAPABLE 1 = PCIe DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

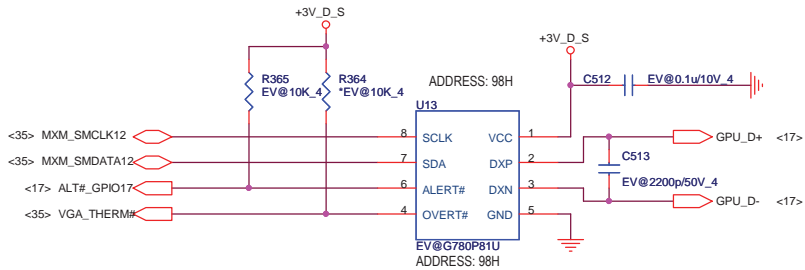
EEPROM(VGA) 5/17 delete EEPROM

DDR3 Memory Aperture size(GPU)

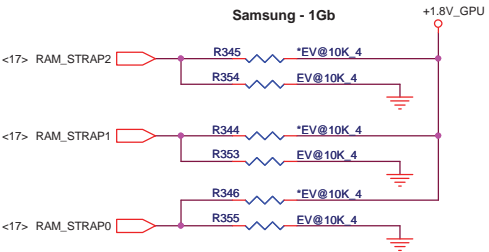
Thermal Sensor(VGA)

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000


USD0.16



DDR3 Memory size					
Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	1	0	1
Samsung					
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128m*16)	0	0	1
AMD					
	23EY2387MA12-SZ	AKD5LGGT700	0	1	0



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.



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Size

Document Number

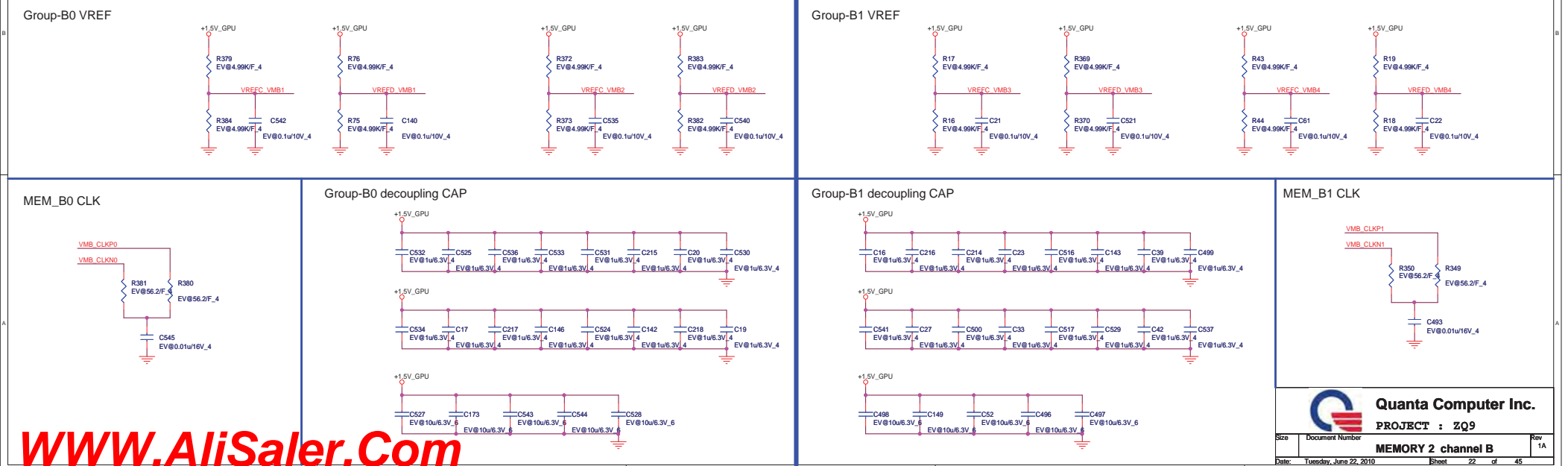
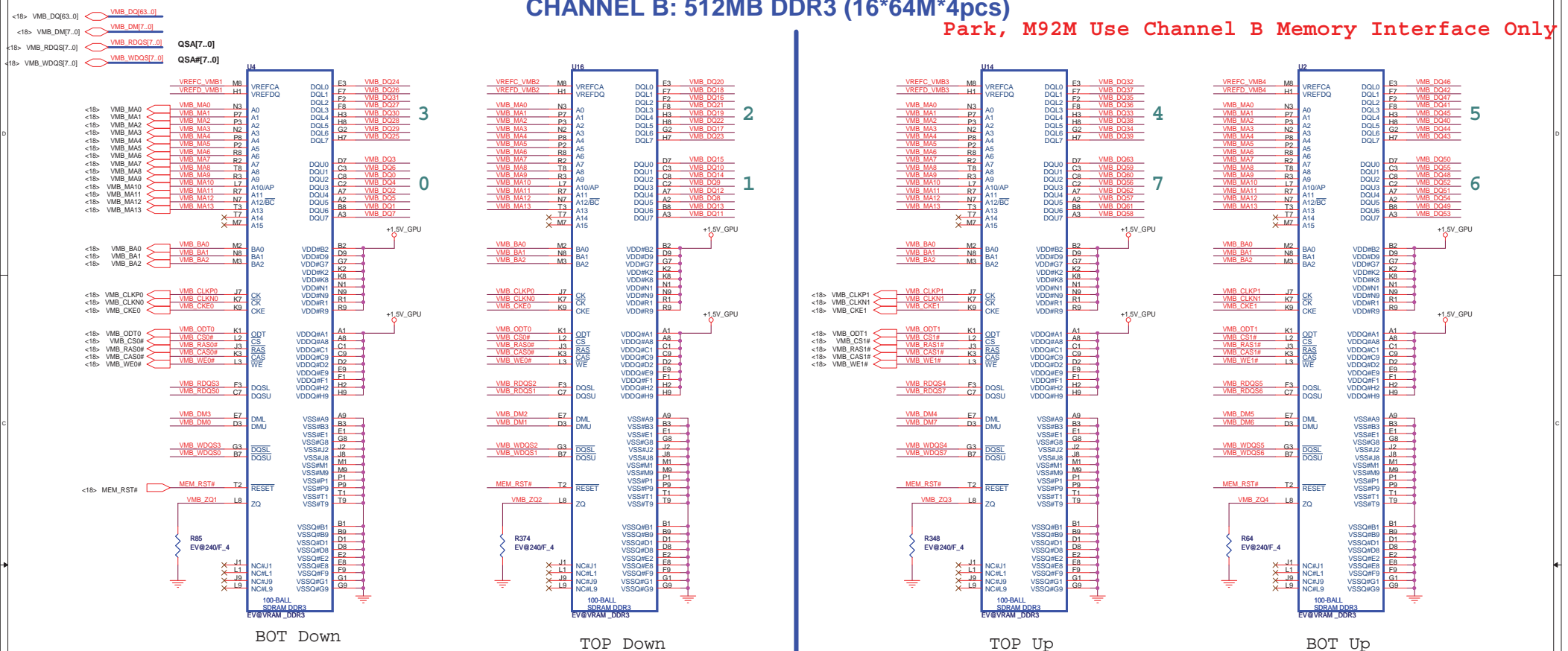
Strip/Thermal

Date: Tuesday, June 22, 2010

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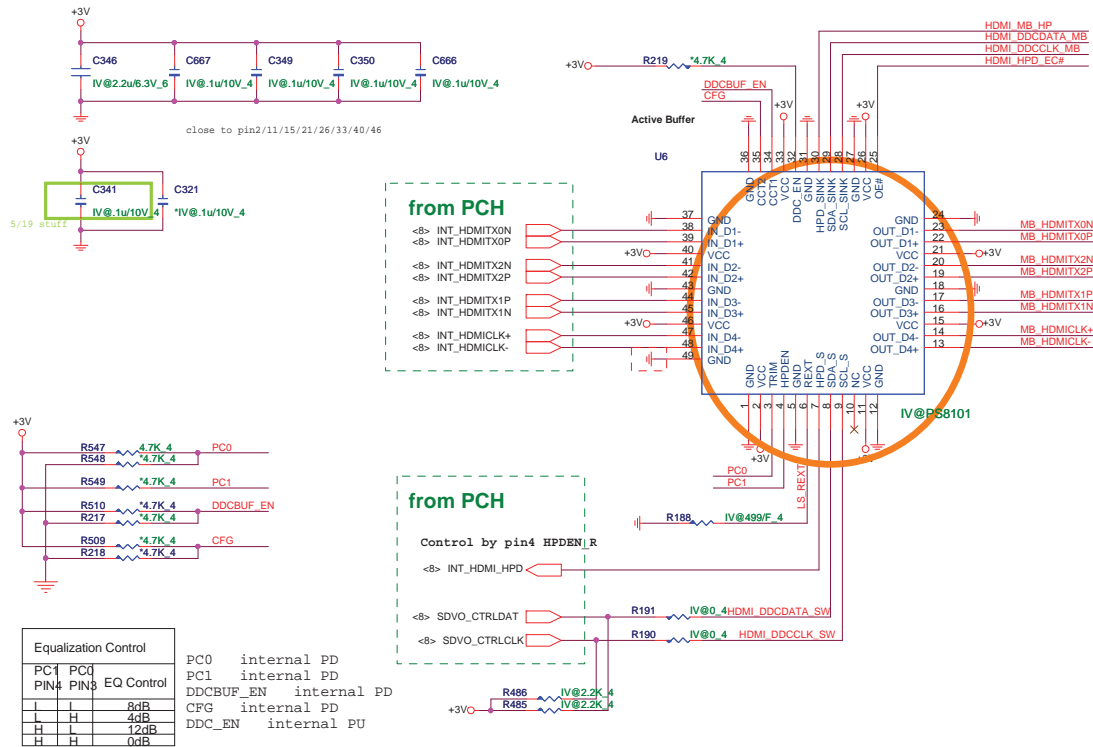
Rev 1A

Park, M92M Use Channel B Memory Interface Only

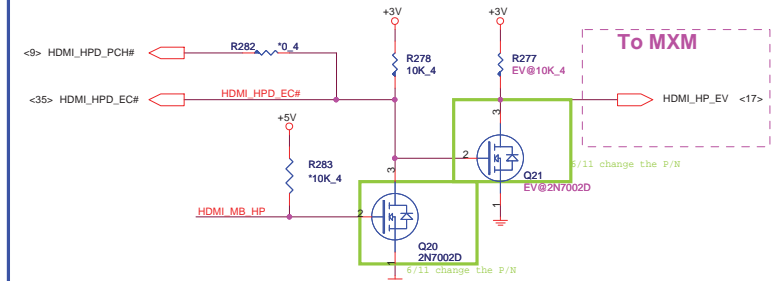


I@ HDMI LEVEL SHIFTER

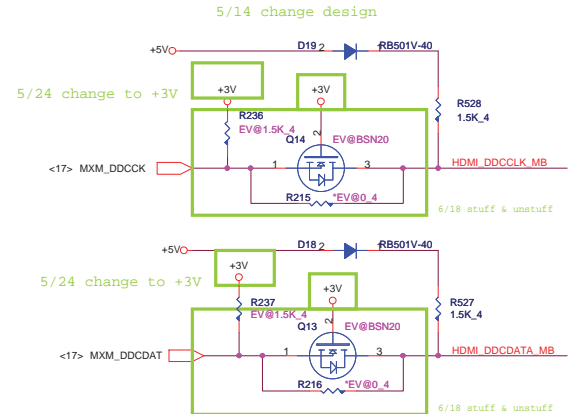
IV@
EV@



SW@HDMI-detect



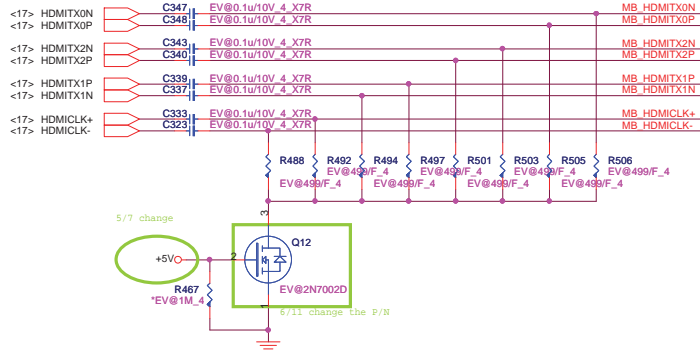
I2C



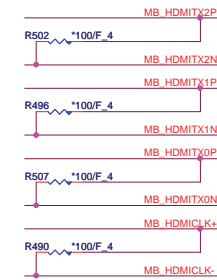
AC-coupling CAP place close to HDMI-connector

Switchable Graphic HDMI source

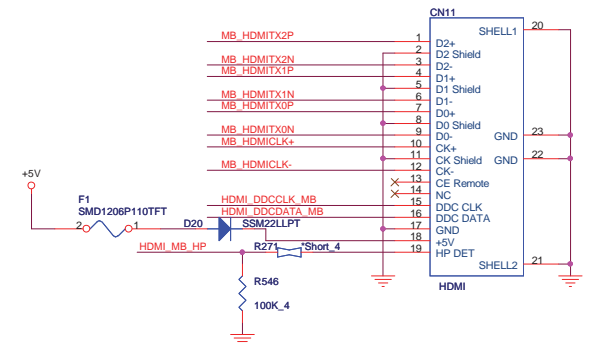
From GPU



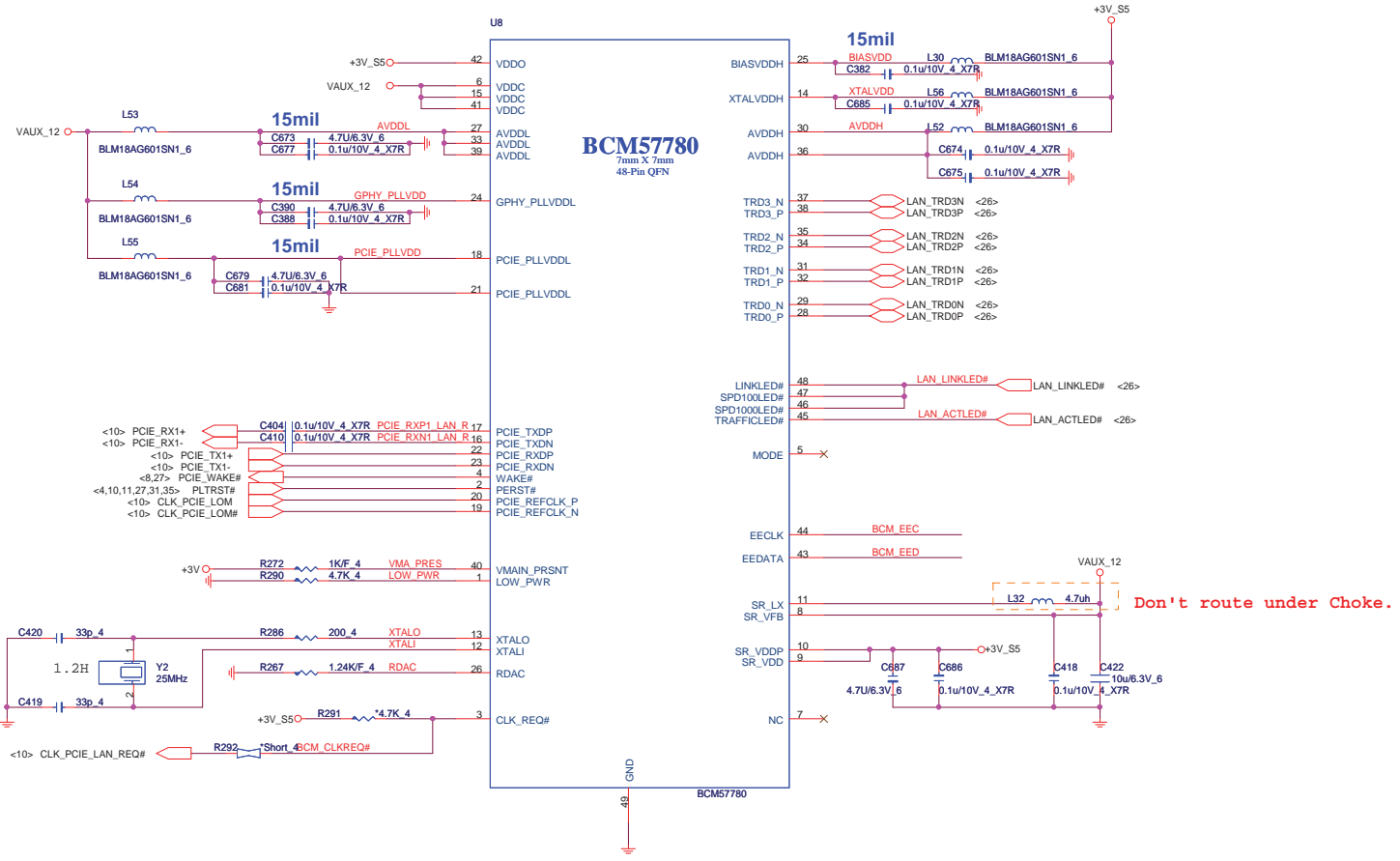
EMI



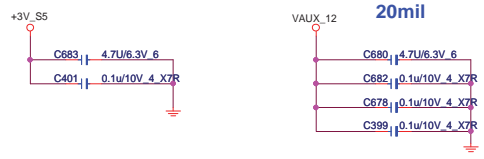
HDMI connector



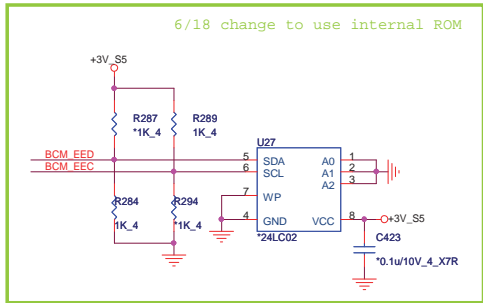
Giga-LAN BCM57780



LAN POWER



EEPROM

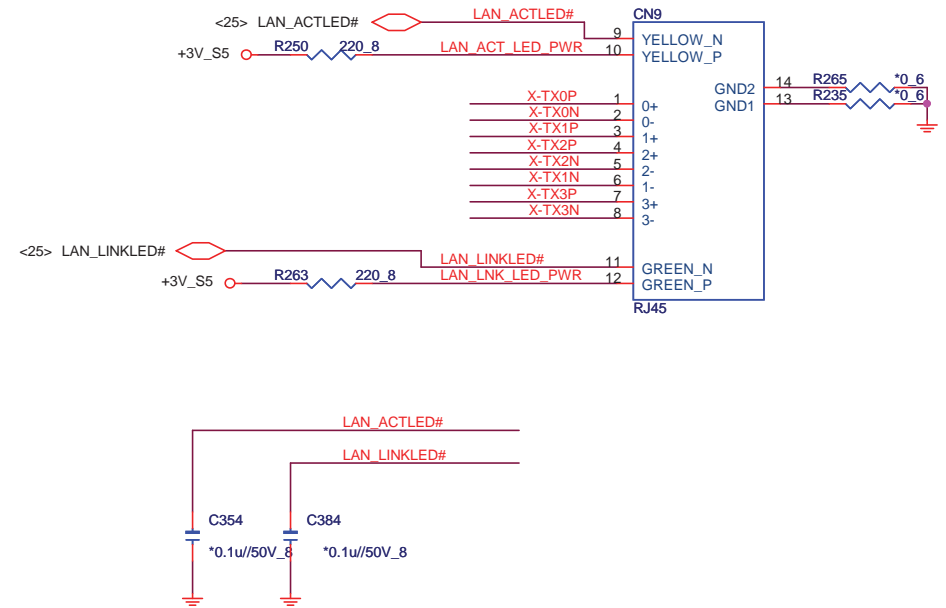


EEPROM Strapping

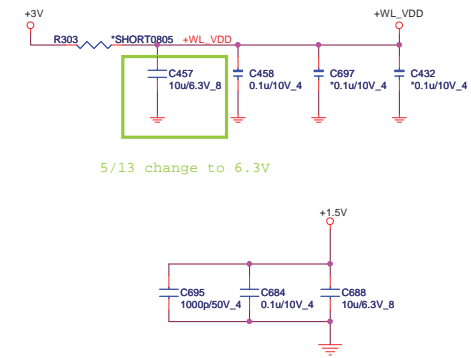
EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

A version Still mount the EEPROM

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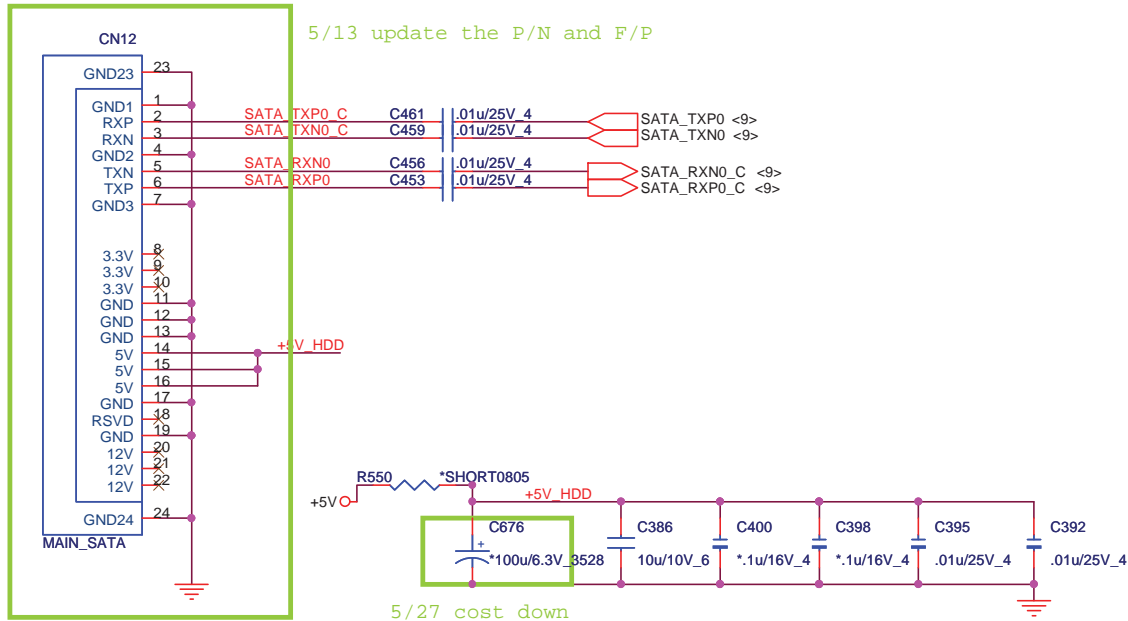


+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



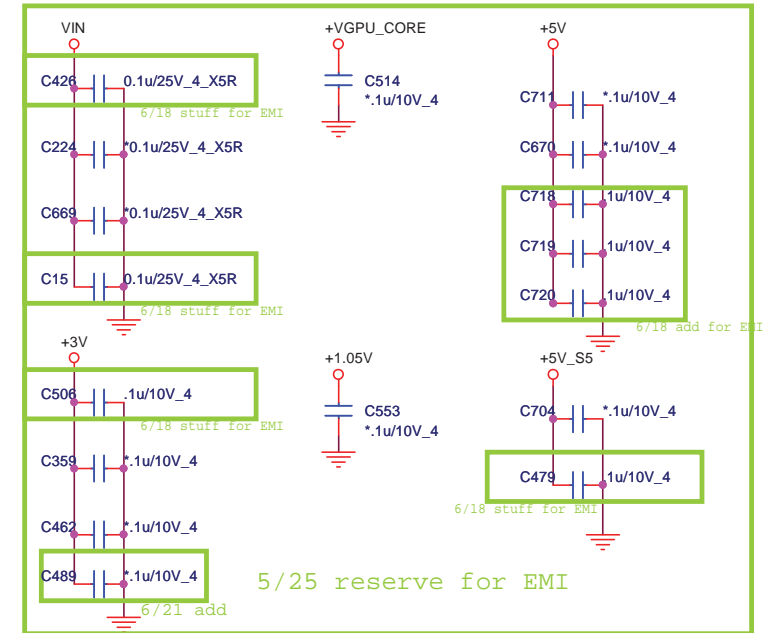
MAIN SATA HDD

5/13 update the P/N and F/P



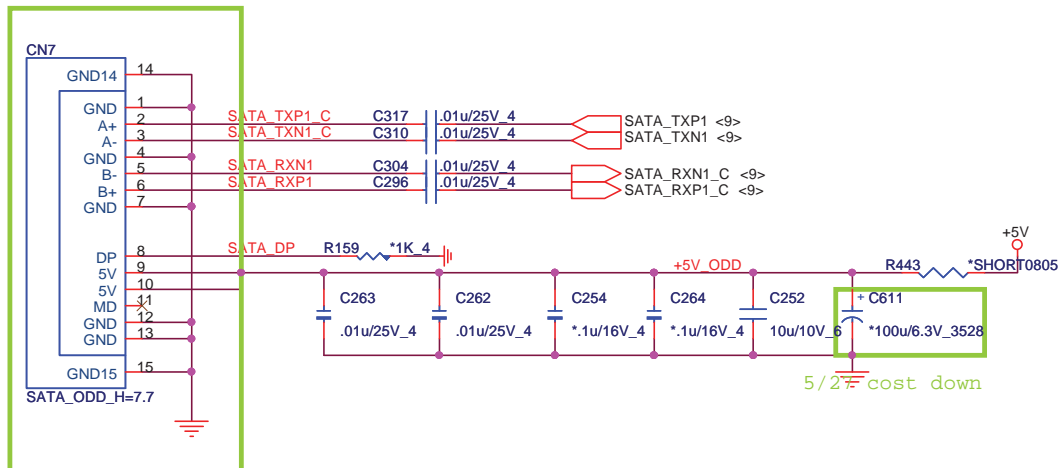
5/27 cost down

EE RETURN-PATH CAPACITORS




5/25 reserve for EMI

ODD (SATA)

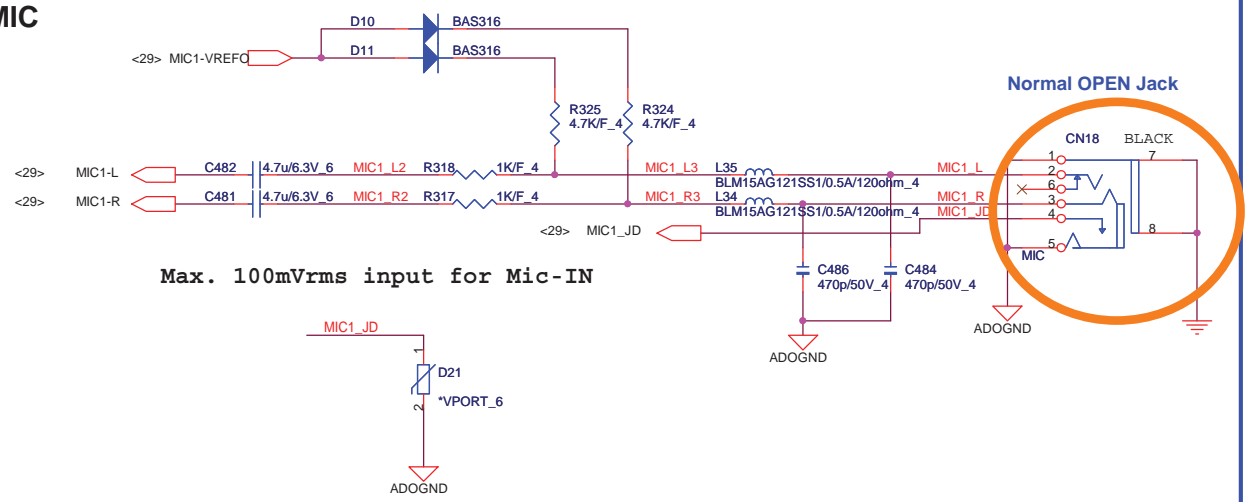


5/27 cost down

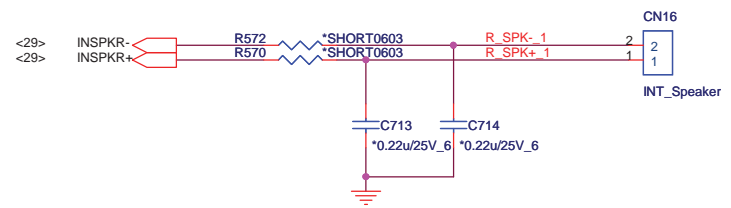
5/26 change the footprint

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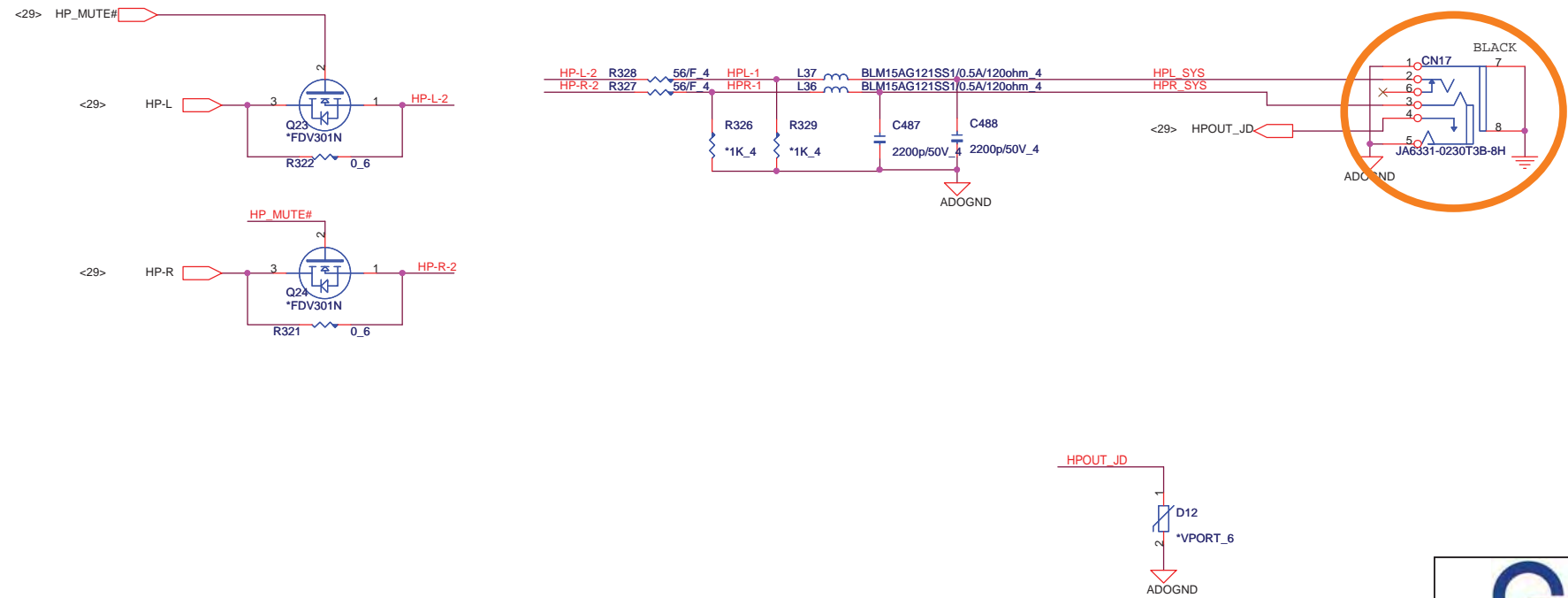
MIC




Internal Speaker



HP/SPDIF





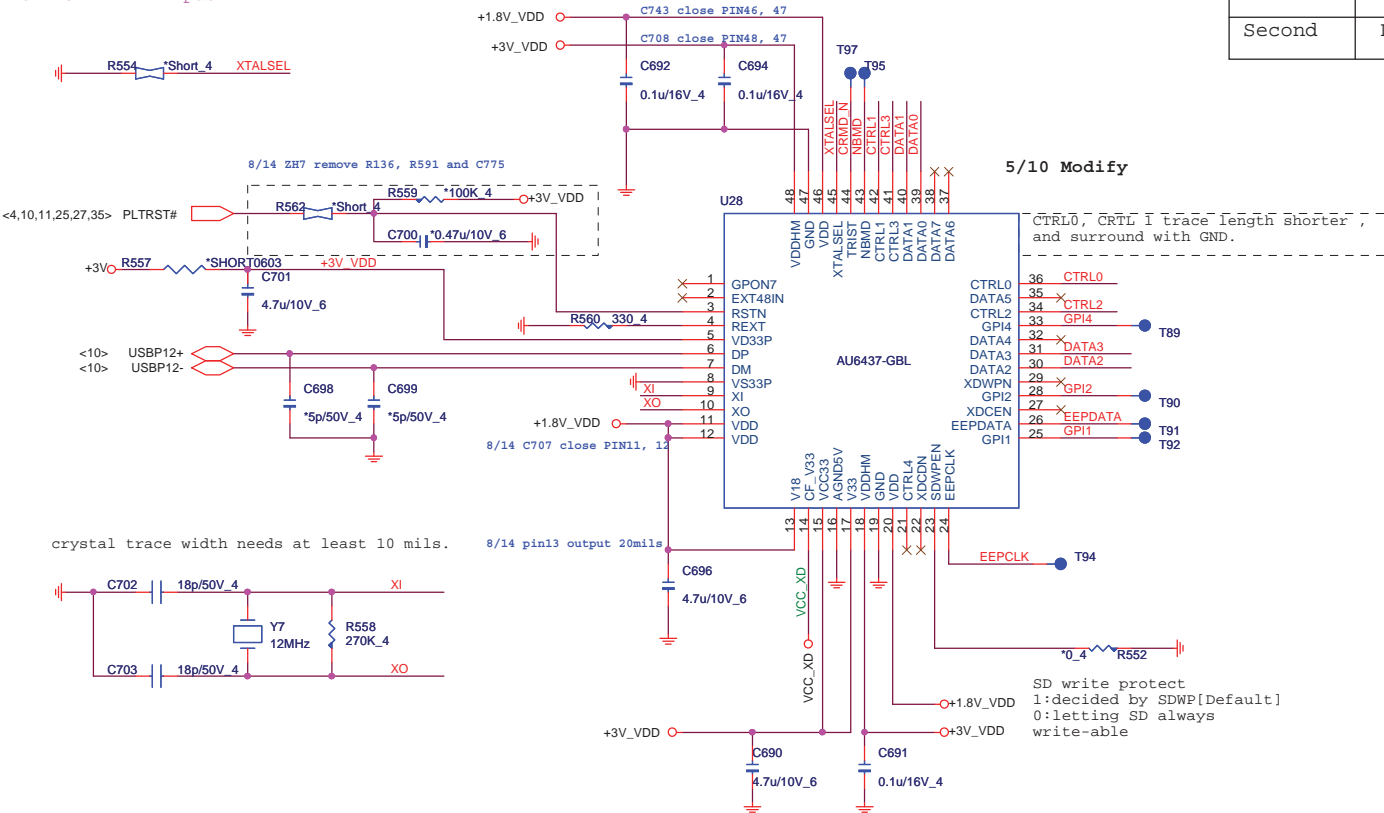
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PROJECT : ZQ9

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		1A
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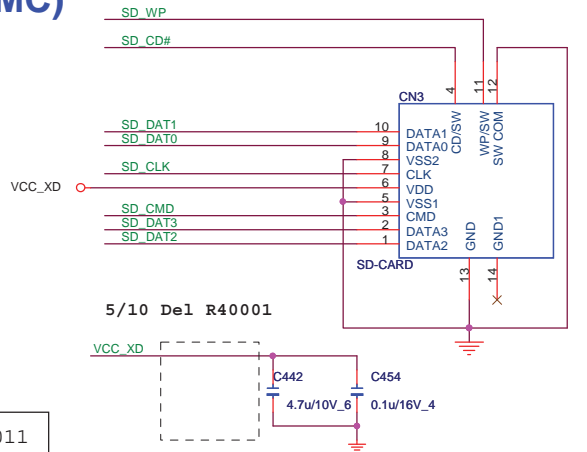
CARD READER Controller

2 IN 1 CARD READER (SD/MMC)

Clock input selection
'1' for 48MHz input [Default, Internal PU]
'0' for 12MHz input



Main	DFHS11FR011
Second	DFHS11FR033

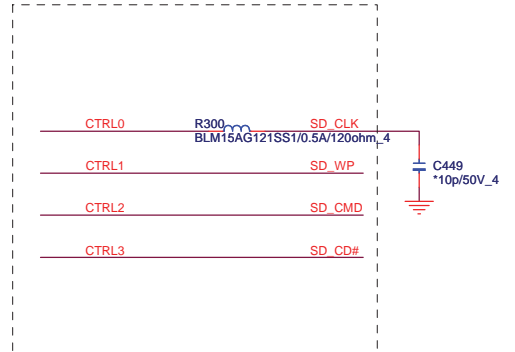


Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

5/10 change Card Redaer conn
footpirnt sdcard-sdsn09-08-xa-11p-smt



Close to connector



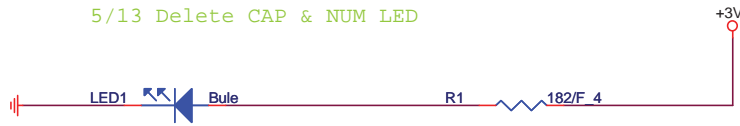
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number AU6433 CardReader	Rev 1A
Date:	Tuesday, June 22, 2010	Sheet 31 of 43

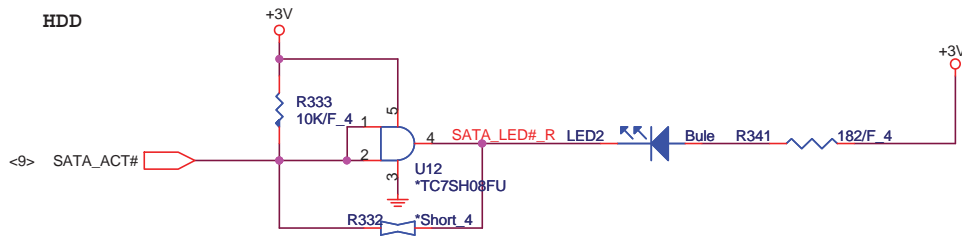
LED

5/13 Delete CAP & NUM LED

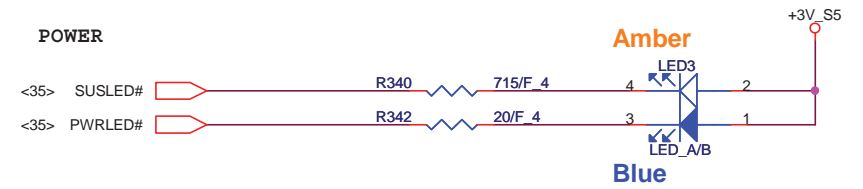
Power LED



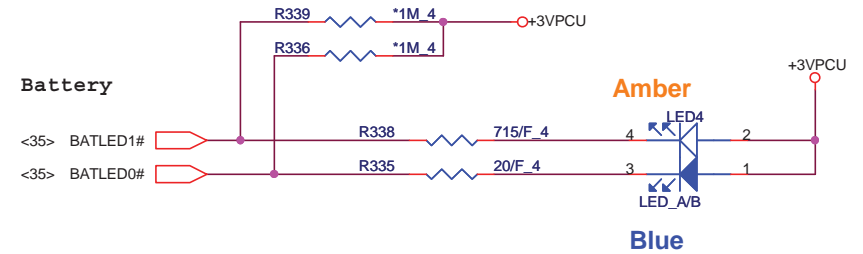
HDD



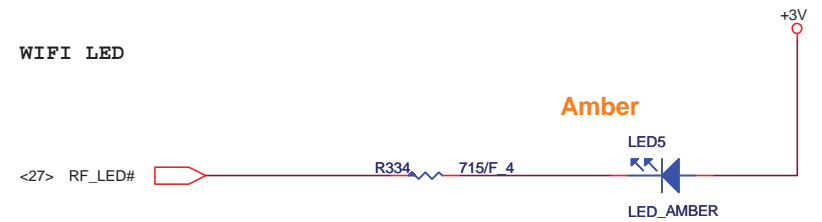
POWER




Battery

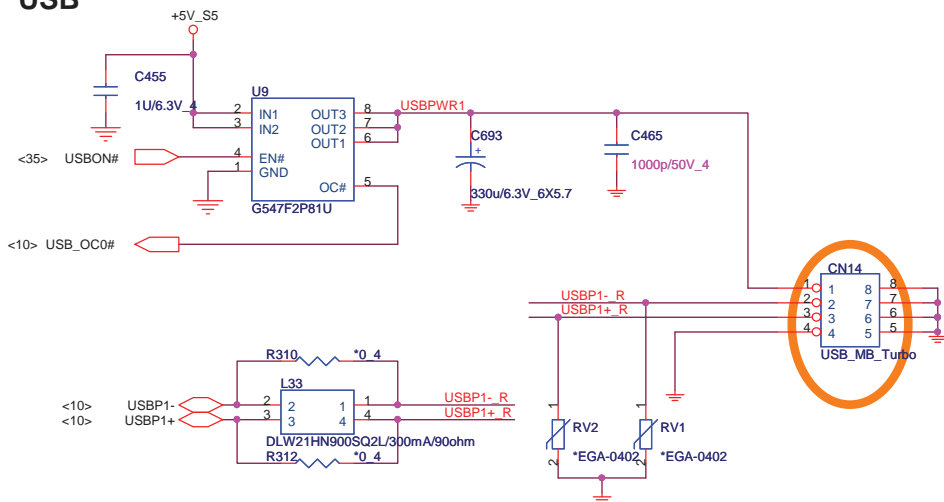


WIFI LED



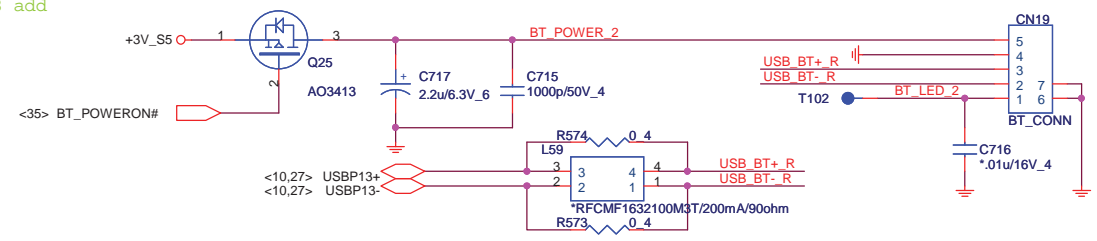
 Quanta Computer Inc. PROJECT : ZQ9		Size	Document Number	Rev 1A
		POWER/MMB/LAUNCH/LED		
Date: Tuesday, June 22, 2010		Sheet 32 of 45		

USB

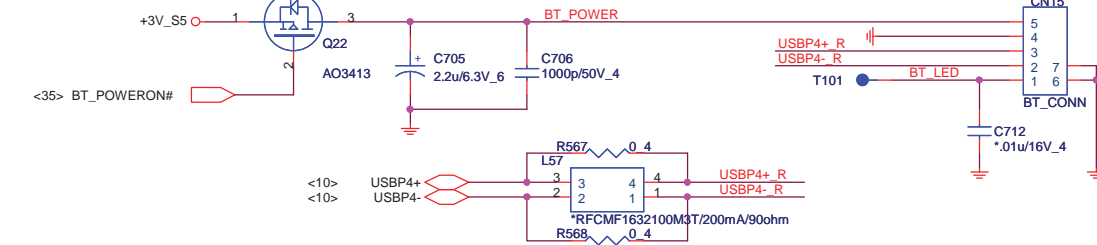


BLUETOOTH CONNECTOR for 2.0

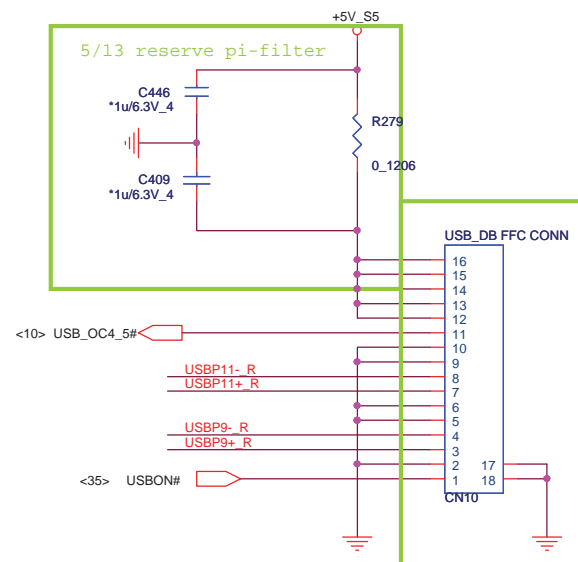
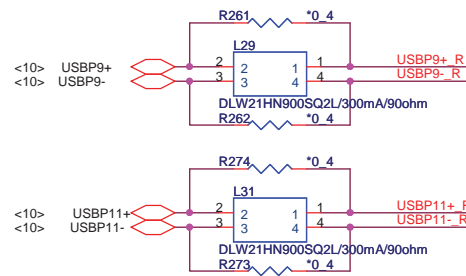
6/18 add



BLUETOOTH CONNECTOR for 3.0



USB/B



5/11 update the footprint



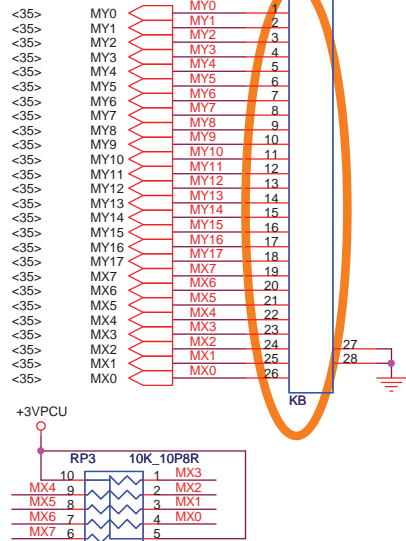
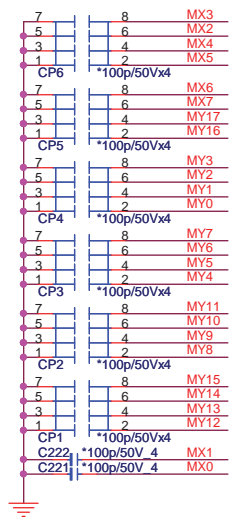
Quanta Computer Inc.

PROJECT : ZQ9

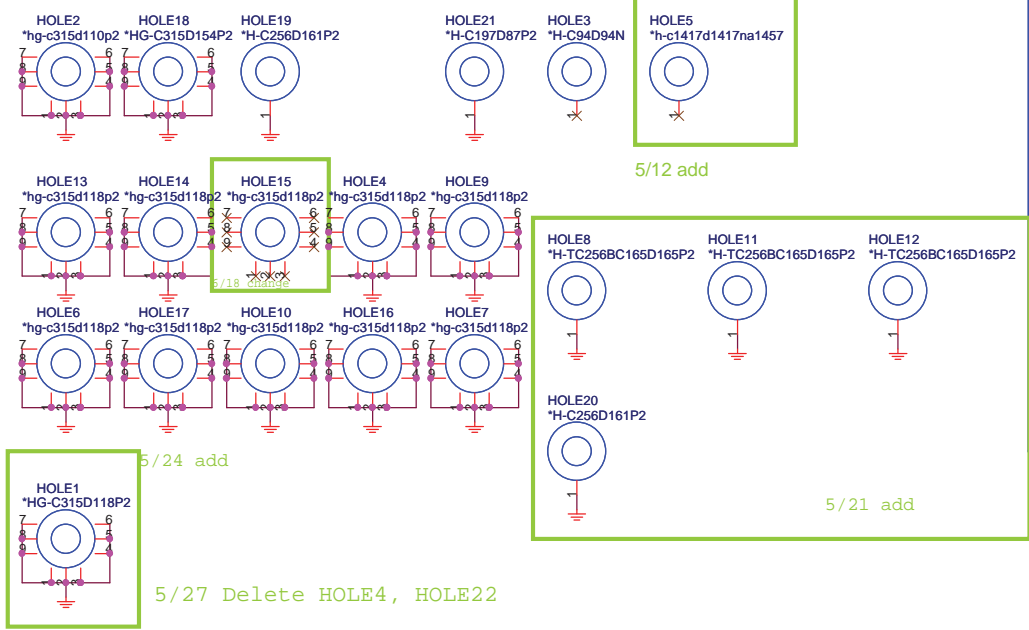
Size	Document Number	Rev
	USB/ BT	1A

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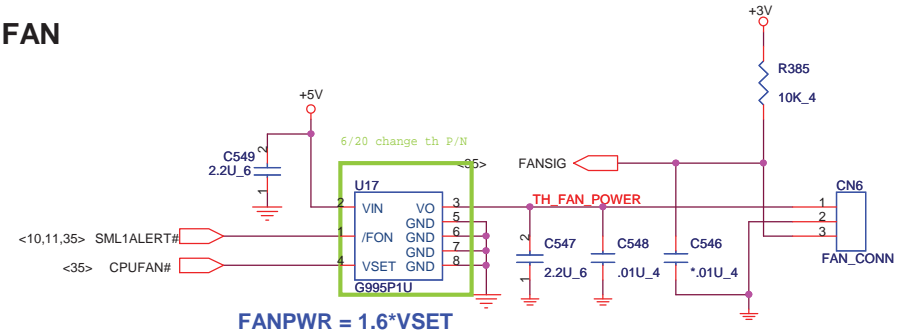
K/B



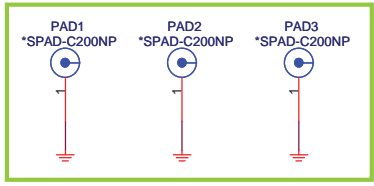
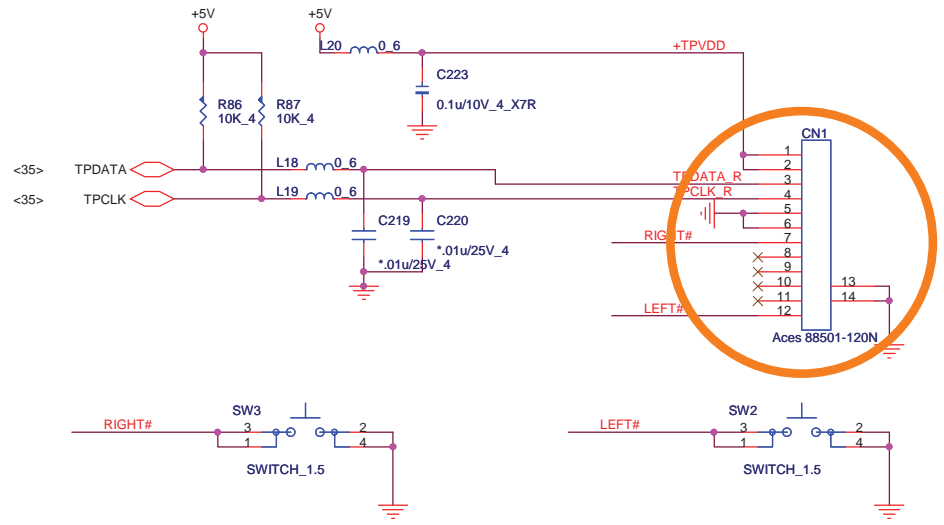
HOLE




CPU FAN



TOUCHPAD & Switch CONN.

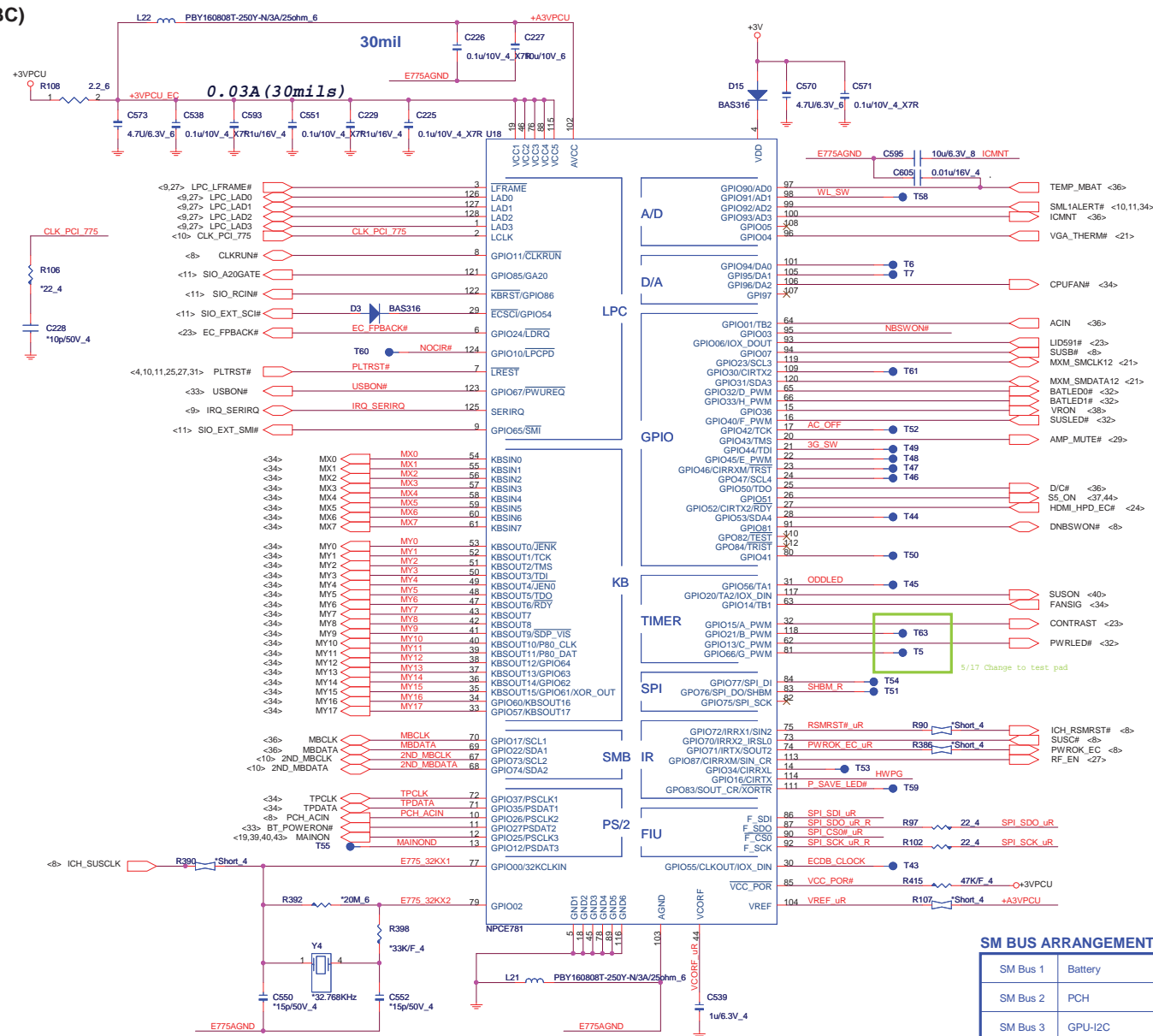




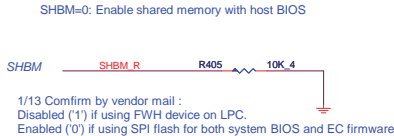
Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	KB/FAN/TP+FP	1A
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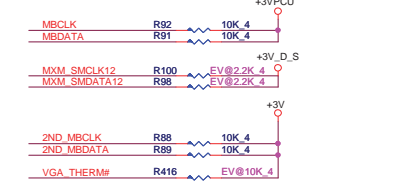
EC(KBC)



I/O ADDRESS SETTING(KBC)



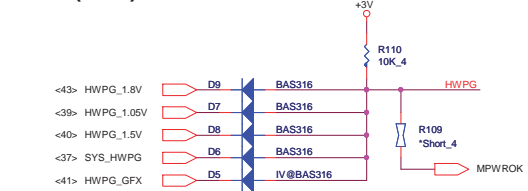
SM BUS PU(KBC)



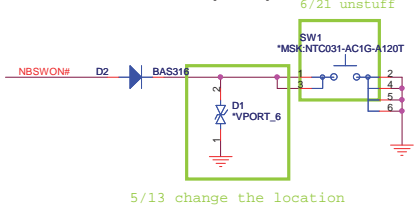
SPI FLASH(KBC)



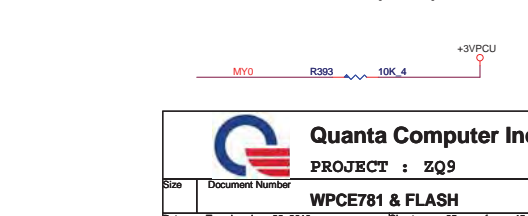
HWPG(KBC)



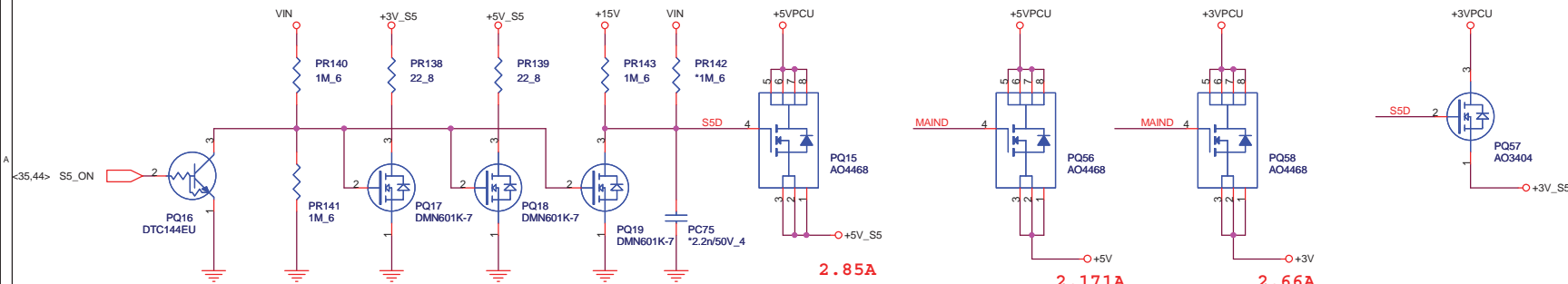
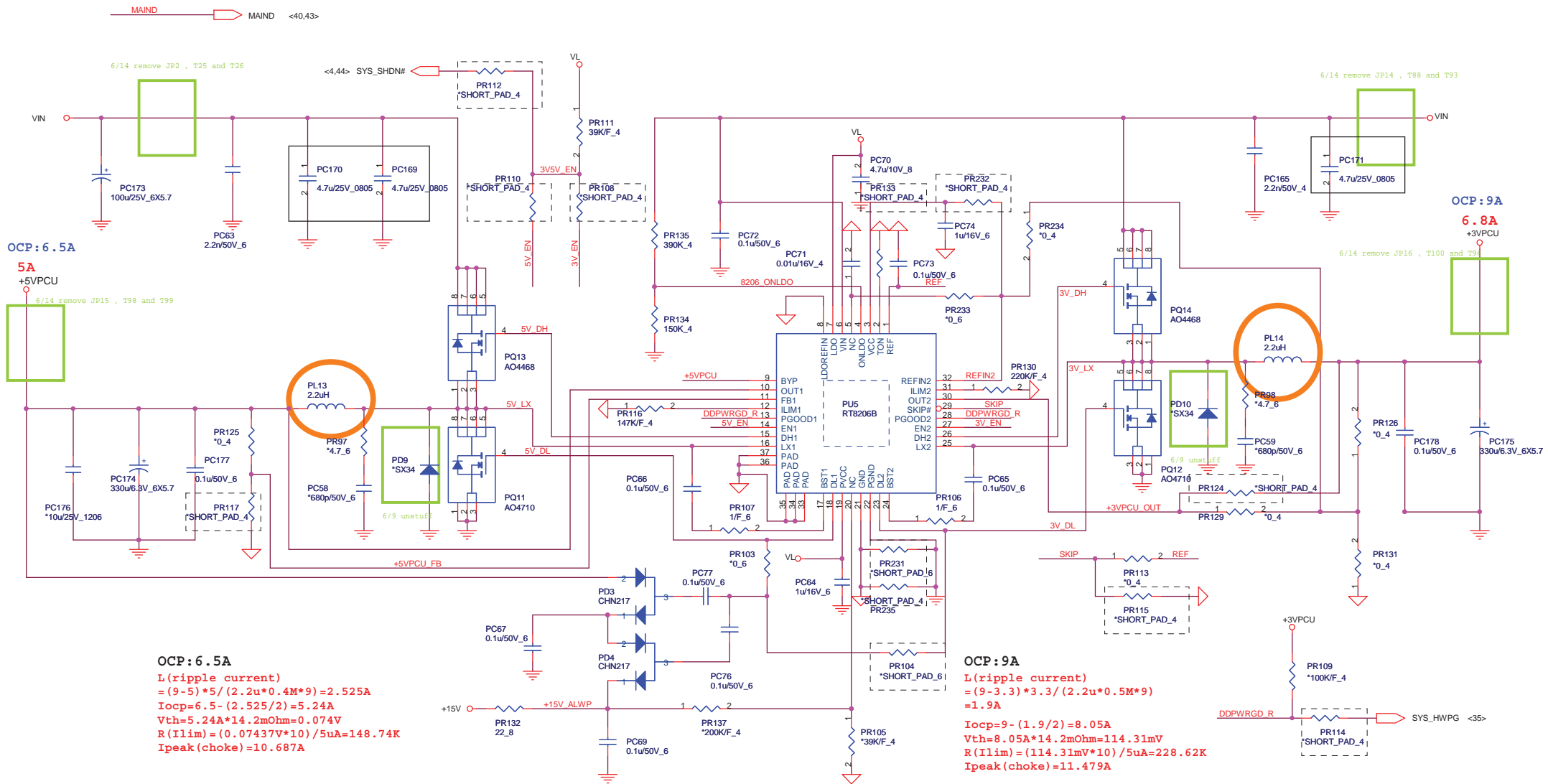
POWER-ON Switch(KBC)

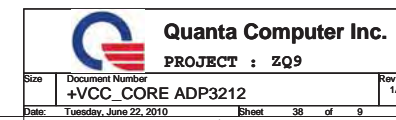


INTERNAL KEYBOARD STRIP SET(KBC)



SM BUS ARRANGEMENT TABLE	
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU-I2C
SM Bus 4	N/A



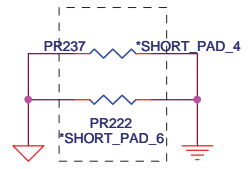



<35> HWPG 1.05V

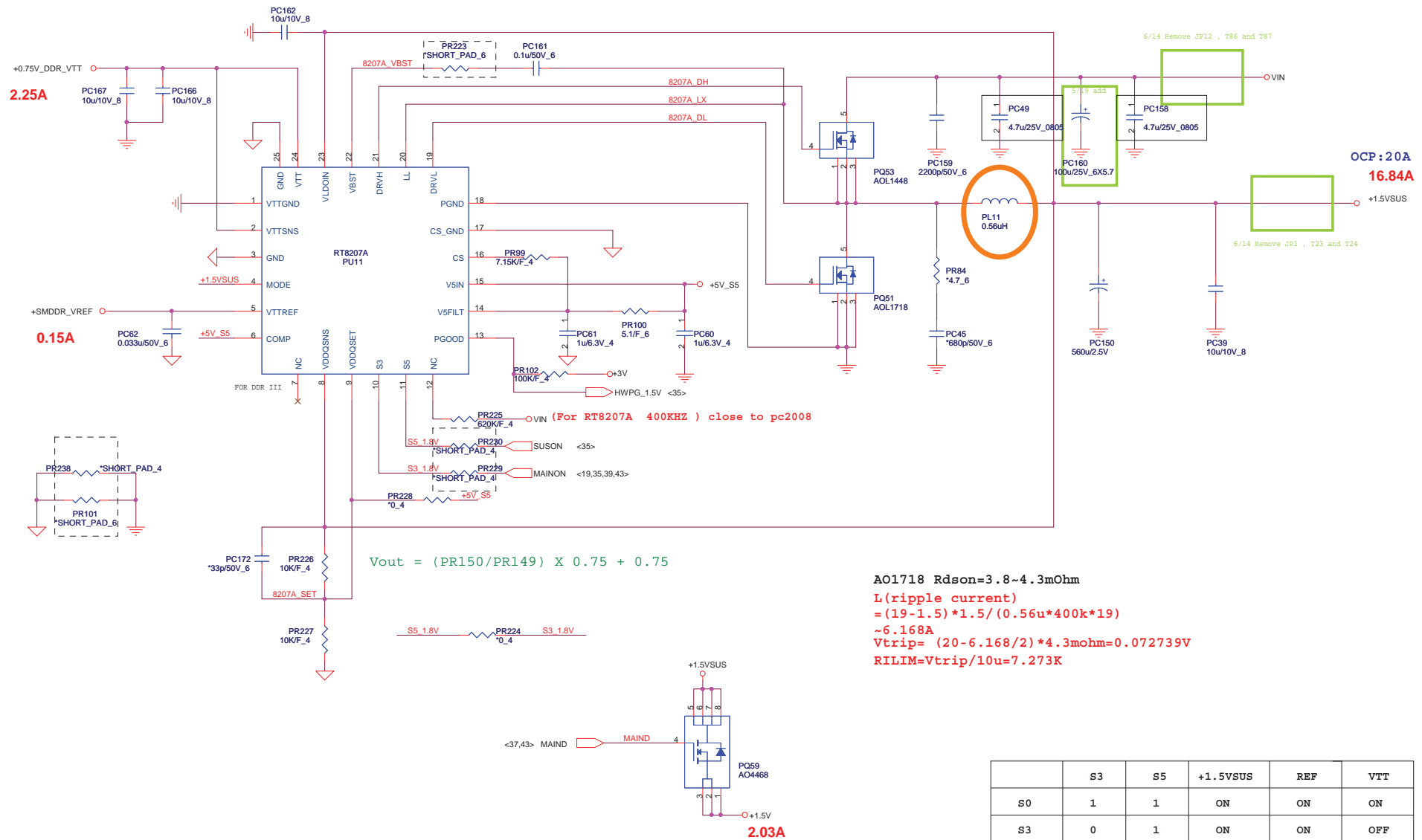


$$\begin{aligned} \text{TON} &= 3.85\text{p} \cdot \text{RTON} \cdot \text{Vout} / (\text{Vin} - 0.5) \\ \text{Frequency} &= \text{Vout} / (\text{Vin} \cdot \text{TON}) \\ \text{TON} &= 3.85\text{p} \cdot 1\text{M} \cdot 1 / (\text{Vin} - 0.5) \\ \text{Frequency} &= 1 / (0.0036767) = 272\text{K} \end{aligned}$$

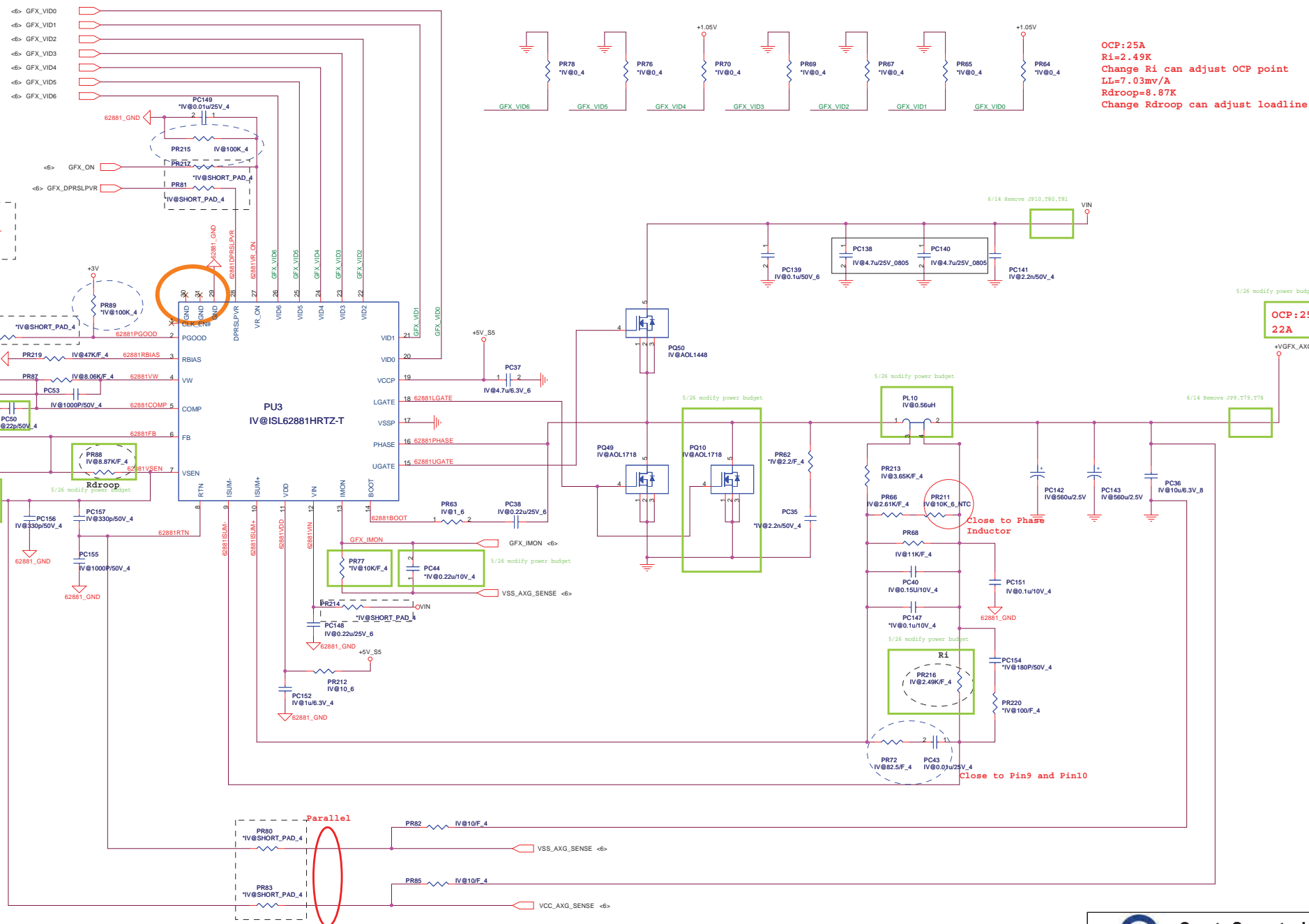
AO1718 R_{dson}=3~4.3mOhm
L(ripple current)
=(19-1.05)*1.05/(0.56u*272k*19)
~6.512A
R_{LIM}=2.15mohm*23-3.256/20uA=2.122Kohm
I(choke)_{peak}=29.512A



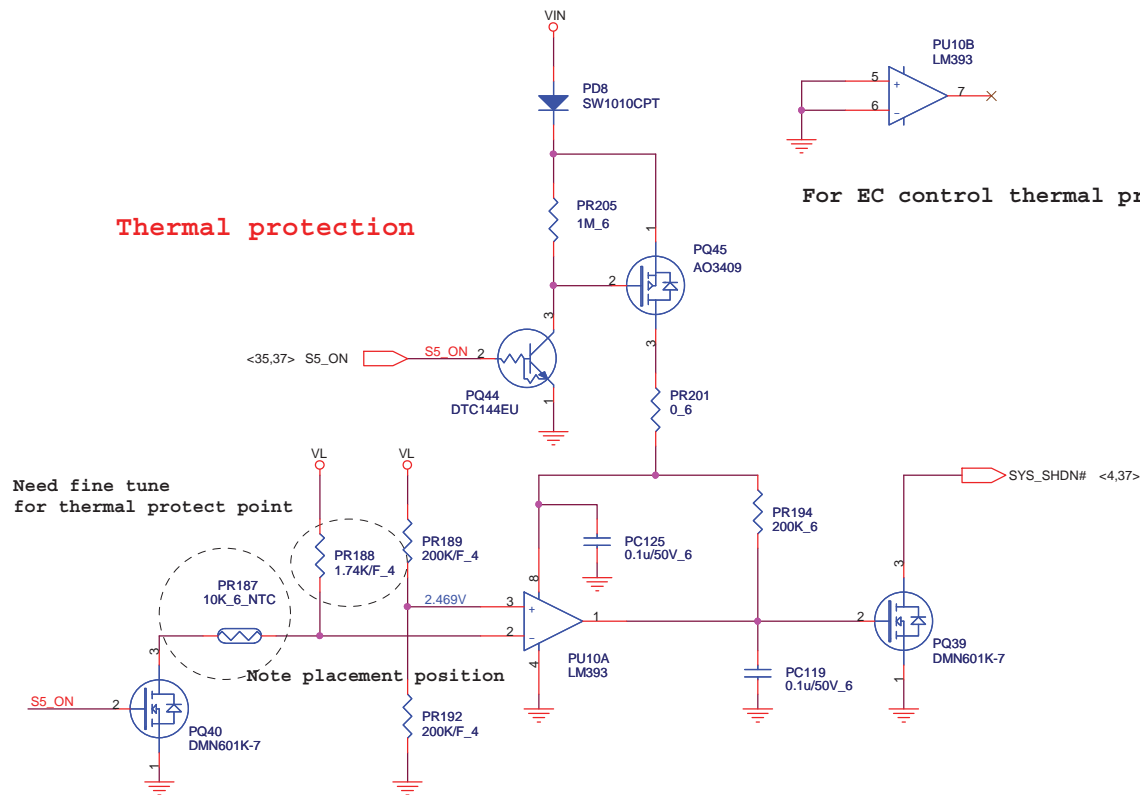
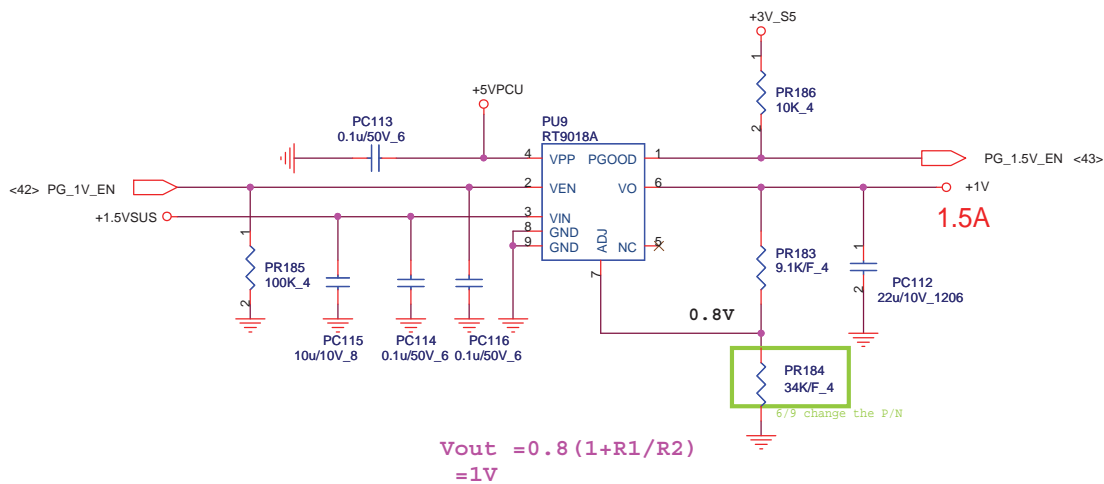
 <div> Quanta Computer Inc. PROJECT : ZQ9 </div>		
Size	Document Number +VTT (UP6111A)	Rev 1A
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	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF







[illegible]